SILICON DARLINGTON POWER TRANSISTORS

NPN silicon Darlington transistors in a SOT186 envelope with an electrically insulated mounting base. PNP complements are BD644F, BD646F, BD648F, BD650F and BD652F.

QUICK REFERENCE DATA

			BD643F	645F	647F	649F	651F	
Collector-base voltage (open emitter)	V_{CBO}	max.	60	80	100	120	140	V
Collector-emitter voltage (open base)	V_{CEO}	max.	45	60	80	100	120	V
Collector current (DC)	I_C	max.			8			A
Total power dissipation at $T_h \leq 25\ ^oC$	P_{tot}	max.			20			W
Junction temperature	T_j	max.			150			^oC

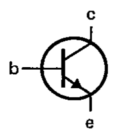
MECHANICAL DATA

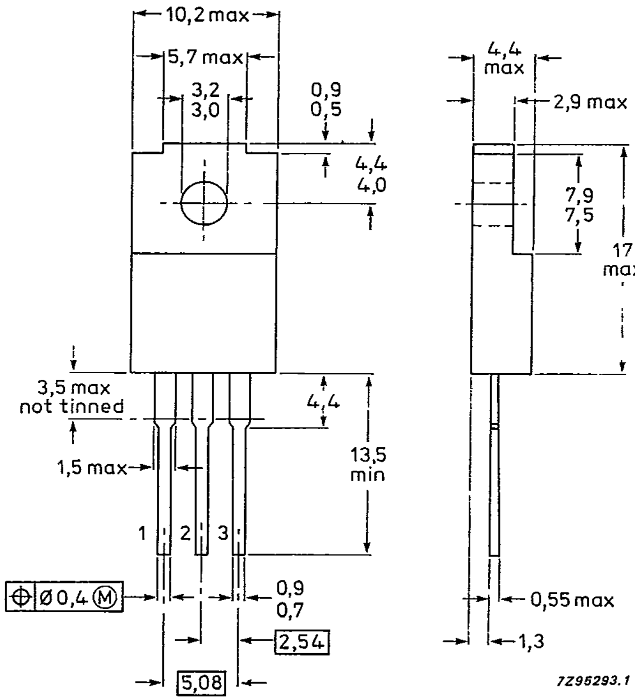
Dimensions in mm

Fig.1 SOT186.

Pinning

1 = base
2 = collector
3 = emitter





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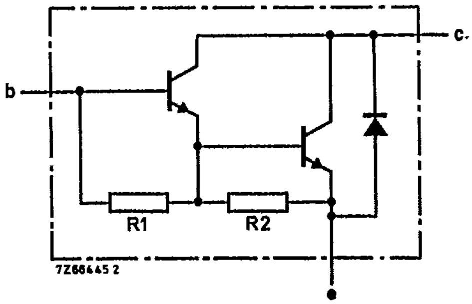

R1 typ. 4 kΩ
R2 typ. 100 kΩ

Fig. 2 Darlington circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BD643F	645F	647F	649F	651F	
Collector-base voltage (open emitter)	V_{CBO}	max.	60	80	100	120	140	V
Collector-emitter voltage (open base)	V_{CEO}	max.	45	60	80	100	120	V
Emitter-base voltage (open collector)	V_{EBO}	max.			5			V
Collector current (DC)	I_C	max.			8			A
(peak value)	I_{CM}	max.			12			A
Base current (DC)	I_B	max.			150			mA
Total power dissipation at $T_h \leq 25\ ^oC$ (note 1)	P_{tot}	max.			20			W
at $T_h \leq 25\ ^oC$ (note 2)	P_{tot}	max.			32			W
Storage temperature range	T_{stg}				−65 to +150			°C
Junction temperature	T_j	max.			150			°C

THERMAL RESISTANCE

From junction to internal heatsink	$R_{th\text{-}jmb}$	=	1.6	K/W
From junction to external heatsink (note 1)	$R_{th\ j\text{-}h}$	=	6.3	K/W
From junction to external heatsink (note 2)	$R_{th\ j\text{-}h}$	=	3.9	K/W

INSULATION

Voltage allowed between all terminals and external heatsink (peak value)	V_{insul}	max.	1000	V
Isolation capacitance from collector to external heatsink	C_{th}	max.	12	pF

Notes

1. Mounted without heatsink compound and 30 ± 5 newtons pressure on centre of envelope.
2. Mounted with heatsink compound and 30 ± 5 newtons pressure on centre of envelope.

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T-33-29

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off currents								
$I_E = 0$; $V_{CB} = V_{CEOmax}$	I_{CBO}	max.			0.1			mA
$I_E = 0$; $V_{CB} = 1/2\ V_{CBOmax}$; $T_j = 150$ °C	I_{CBO}	max.			1			mA
$I_B = 0$; $V_{CE} = 1/2\ V_{CEOmax}$	I_{CEO}	max.			0.2			mA
Emitter cut-off current								
$V_{BE} = 5$ V; $I_C = 0$	I_{EBO}	max.			5			mA

			BD643F	645F	647F	649F	651F	
Static forward current transfer ratio (note 1)								
$I_C = 0.5$ A; $V_{CE} = 3$ V	h_{FE}	typ.	1900	1900	1900	1900	1900	
$I_C = 4$ A; $V_{CE} = 3$ V	h_{FE}	min.	750	—	—	—	—	
$I_C = 3$ A; $V_{CE} = 3$ V	h_{FE}	min.	—	750	750	750	750	
$I_C = 8$ A; $V_{CE} = 3$ V	h_{FE}	typ.	1800	1800	1800	1800	1800	
Collector-emitter saturation voltage (note 1)								
$I_C = 4$ A; $I_B = 16$ mA	V_{CEsat}	max.	2	—	—	—	—	V
$I_C = 3$ A; $I_B = 12$ mA	V_{CEsat}	max.	—	2	2	2	2	V
$I_C = 5$ A; $I_B = 50$ mA	V_{CEsat}	max.	2.5	2.5	2.5	2.5	2.5	V
Base-emitter saturation voltage (note 1)								
$I_C = 5$ A; $I_B = 50$ mA	V_{BEsat}	max.	3	3	3	3	3	V
Base-emitter voltage (note 1)								
$I_C = 4$ A; $V_{CE} = 3$ V	V_{BE}	max.	2.5	—	—	—	—	V
$I_C = 3$ A; $V_{CE} = 3$ V	V_{BE}	max.	—	2.5	2.5	2.5	2.5	V
Common-emitter cut-off frequency								
$I_C = 4$ A; $V_{CE} = 3$ V	f_{hfe}	typ.	50	—	—	—	—	kHz
$I_C = 3$ A; $V_{CE} = 3$ V	f_{hfe}	typ.	—	50	50	50	50	kHz
Small signal current gain								
$I_C = 4$ A; $V_{CE} = 3$ V; f = 1 MHz	h_{fe}	typ.	10	—	—	—	—	
$I_C = 3$ A; $V_{CE} = 3$ V; f = 1 MHz	h_{fe}	typ.	—	10	10	10	10	

Forward bias second breakdown collector current				
$V_{CE} = 50$ V; $t_p = 0.1$ s	$I_{(SB)}$	min.	0.55	A
Forward voltage				
$I_F = 3$ A	V_F	typ.	0.9	V
Switching times				
$I_C = 3$ A; $I_{B\,on} = I_{B\,off} = 12$ mA				
Turn on time	t_{on}	max.	2	μs
		typ.	1	μs
Turn off time	t_{off}	max.	10	μs
		typ.	5	μs

Note

1. To be measured under pulsed conditions, $t_p < 300$ μs; $\delta < 2\%$.

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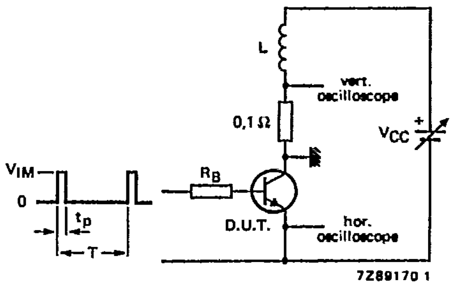
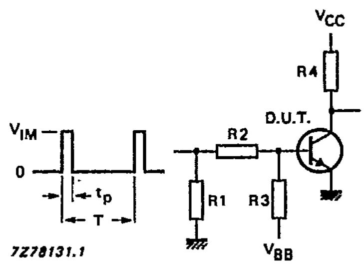


V_{IM} = 12 V
R_B = 270 Ω
L = 5 mH
I_{CC} = 4.5 A
δ = $t_p/T \times 100\%$

Fig. 3 Test circuit for turn-off breakdown energy.



V_{IM} = 10 V
V_{CC} = 10 V
$-V_{BB}$ = 4 V
R_1 = 56 Ω
R_2 = 410 Ω
R_3 = 560 Ω
R_4 = 3 Ω
$t_r = t_f$ = 15 ns
t_p = 10 μs
T = 500 μs

Fig. 4 Switching times test circuit.

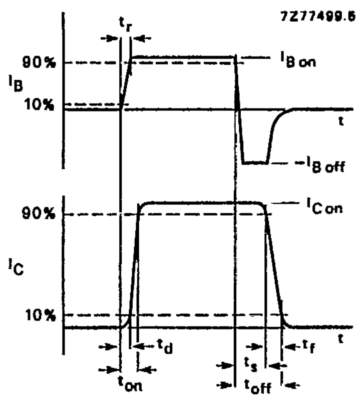
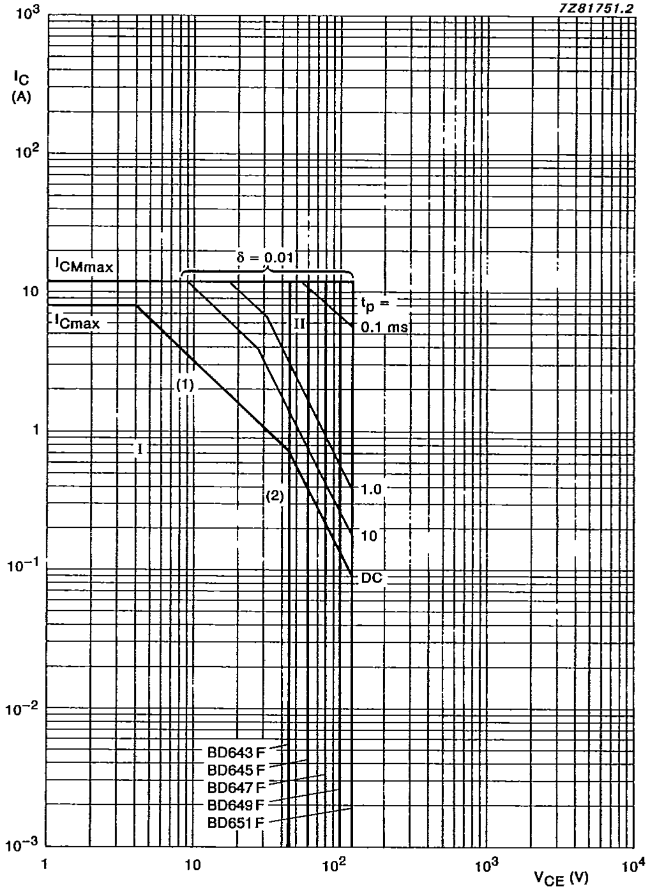


Fig. 5 Switching times waveforms.



I Region of permissible DC operation.
II Permissible extension for repetitive pulse operation.

(1) $P_{tot\ max}$ and P_{peak} lines.
(2) Second-breakdown limits.

Mounted with heatsink compound and 30 ± 5 newtons pressure on centre of envelope.

Fig.6 Safe Operating Area; T_{amb} = 25 °C.

T-33-29

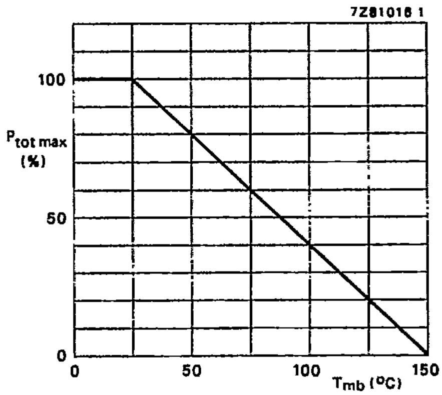


Fig. 7 Power derating curve.

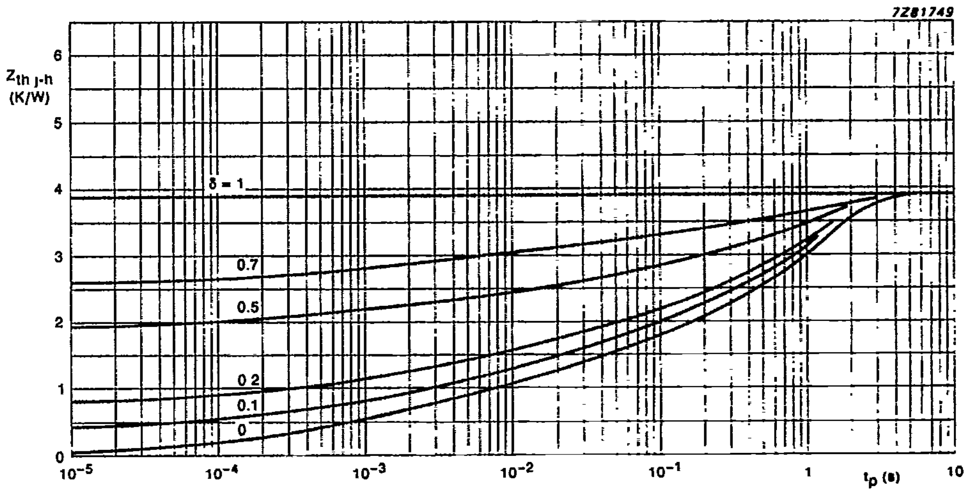


Fig. 8 Pulse power rating chart.

T-33-29

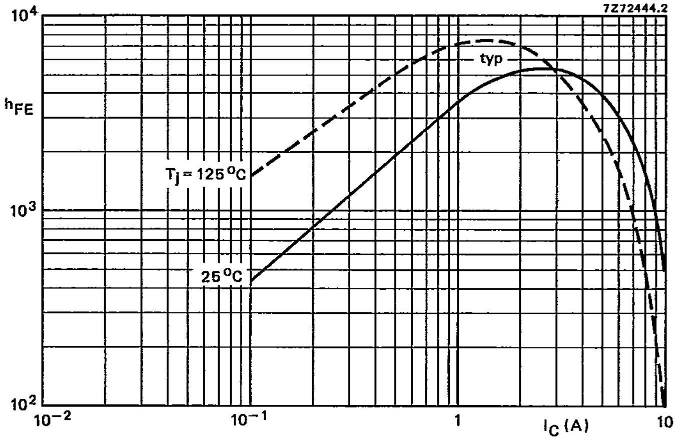


Fig. 9 Typical DC current gain curves; V_{CE} = 3 V.

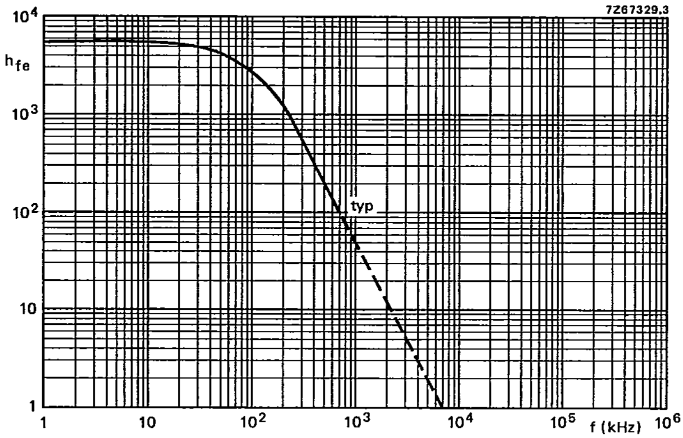


Fig. 10 Small signal current gain.

T-33-29

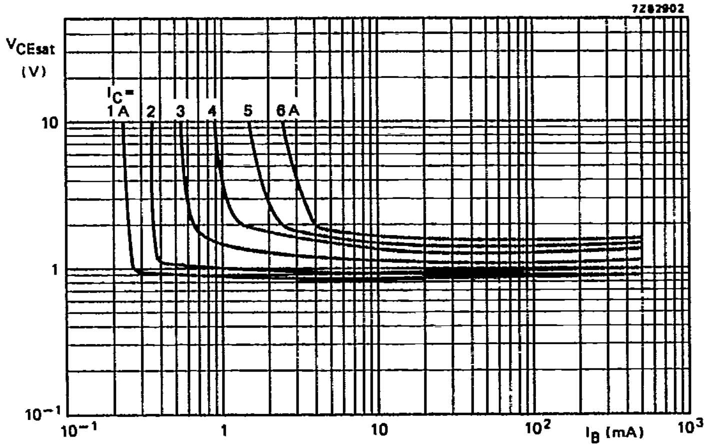


Fig. 11 Typical collector-emitter saturation voltage; $T_j = 25\ ^oC$.