

CMOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

■ CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

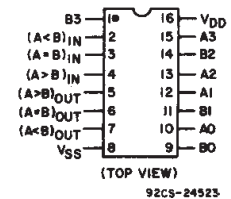
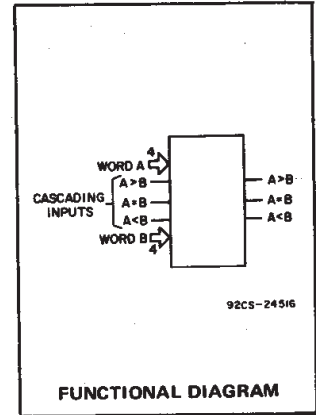
The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix). This device is pin-compatible with the standard 7485 TTL type.

Features:

- Expansion to 8, 12, 16...4N bits by cascading units
- Medium-speed operation:
compares two 4-bit words
in 250 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range) = 1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Servo motor controls
- Process controllers



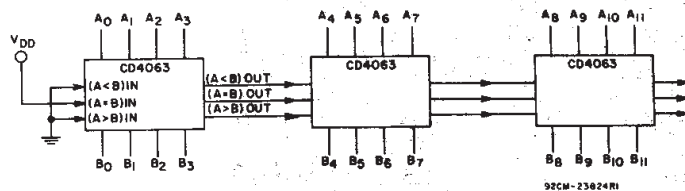
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
Voltages referenced to V_{SS} Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s.max	$+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)	3	18	V



$$t_{p\text{ TOTAL}} = t_{p\text{ (COMPARE)}} + 2 \times t_{p\text{ (CASCADE)}} \text{ AT } V_{DD} = 10\text{V}$$

(3 STAGES)

$$= 250 + (2 \times 200) = 650 \text{ ns (TYP.)}$$

Fig. 1 - Typical speed characteristics of a 12-bit comparator.

CD4063B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5, 13,5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5, 13,5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care

Logic 1 ≡ High Level

Logic 0 ≡ Low Level

CD4063B Types

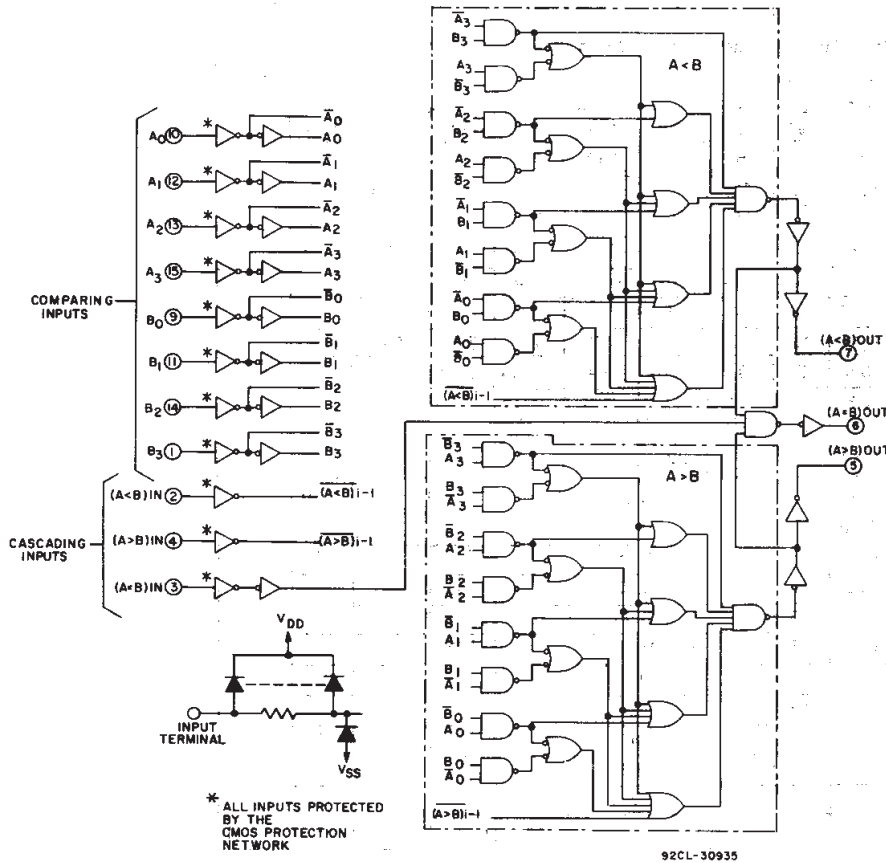


Fig. 2 - Logic diagram for CD4063B.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V _{DD} Volts	Typ.		Max.
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}		5	625	1250	ns
		10	250	500	
		15	175	350	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}		5	500	1000	ns
		10	200	400	
		15	140	280	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF	

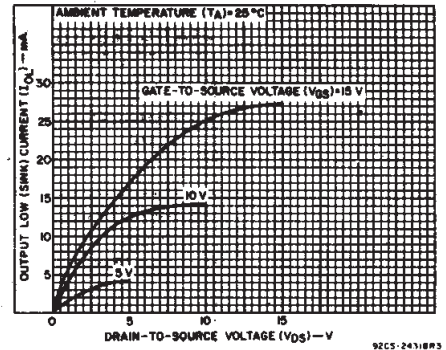


Fig. 3 - Typical output low (sink) current characteristics.

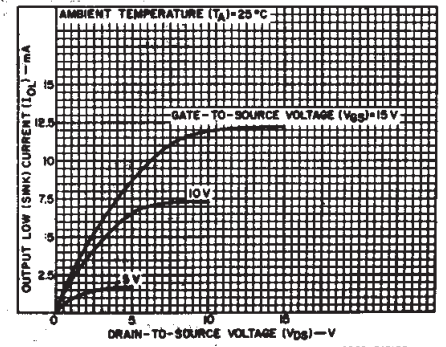


Fig. 4 - Minimum output low (sink) current characteristics.

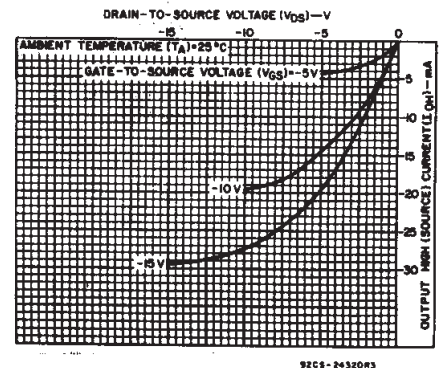


Fig. 5 - Typical output high (source) current characteristics.

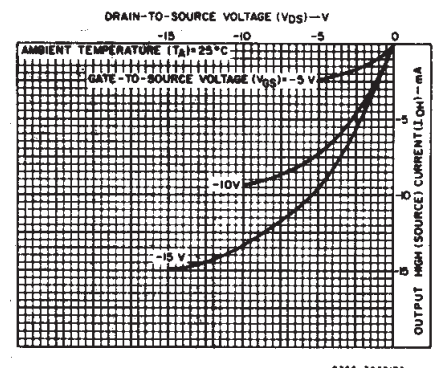


Fig. 6 - Minimum output high (source) current characteristics.

CD4063B Types

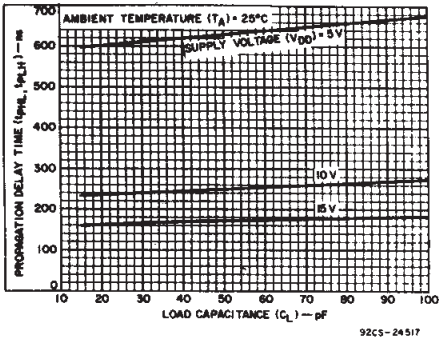


Fig. 7 - Typical propagation delay time vs. load capacitance ("comparing inputs" to outputs).

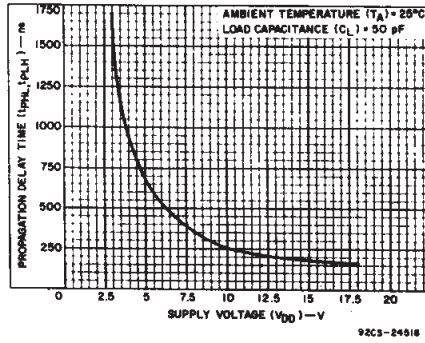


Fig. 8 - Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

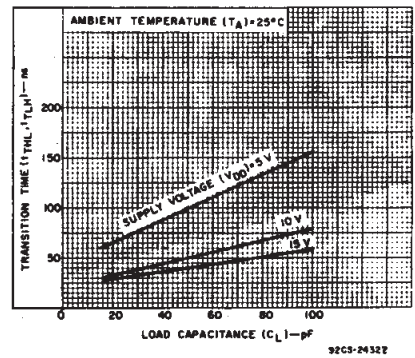


Fig. 9 - Typical transition time vs. load capacitance.

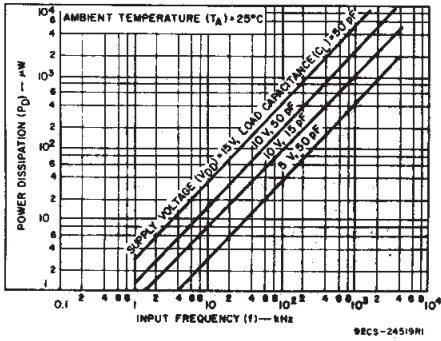


Fig. 10 - Typical power dissipation vs. frequency (see Fig. 12 - dynamic power dissipation test circuit).

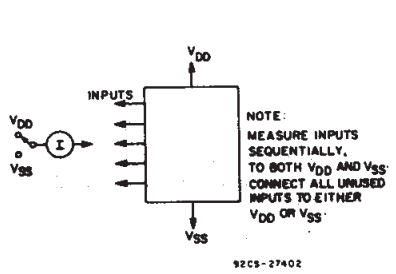


Fig. 11 - Input current test circuit.

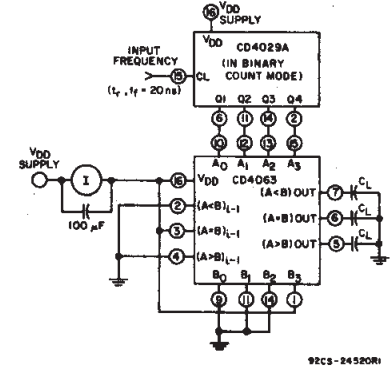


Fig. 12 - Dynamic power dissipation test circuit.

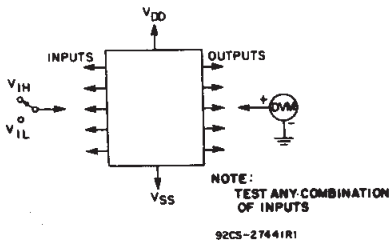


Fig. 13 - Input-voltage test circuit.

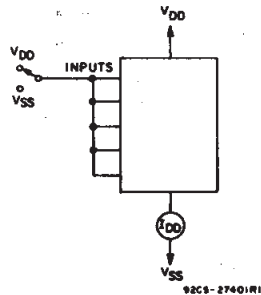
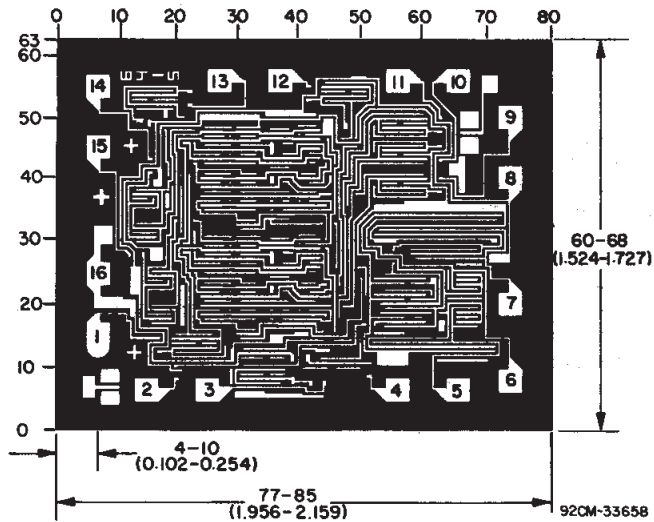


Fig. 14 - Quiescent-device-current test circuit.



Dimensions and pad layout for CD4063BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COMMERCIAL CMOS HIGH VOLTAGE ICs

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.