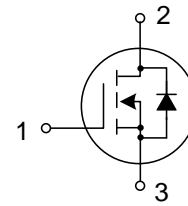
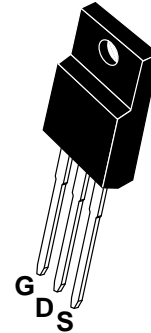


## PIN Connection TO-220F



### Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR10N60F = Specific Device Code

## General Description

FIR10N60FG is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

## Features

- 10A, 600V,  $R_{DS(on)(typ.)} = 0.75\Omega @ V_{GS} = 10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

## Absolute Maximum Ratings (Ta = 25°C unless otherwise noted )

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		$V_{DS}$	600	V
Gate-Source Voltage		$V_{GS}$	±30	V
Drain Current	$T_C = 25^\circ C$	$I_D$	10	A
	$T_C = 100^\circ C$		7	
Drain Current Pulsed		$I_{DM}$	40	A
Power Dissipation ( $T_C = 25^\circ C$ ) -Derate above 25°C		$P_D$	50	W
			0.4	W/°C
Single Pulsed Avalanche Energy (Note 1)		$E_{AS}$	654	mJ
Operation Junction Temperature Range		$T_J$	-55 ~ +150	°C
Storage Temperature Range		$T_{stg}$	-55 ~ +150	°C

**Thermal Characteristics**

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	$^{\circ}C/W$

**Electrical Characteristics (Ta = 25°C unless otherwise noted)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{VDSS}$	25 °C, $V_{GS}=0V$ , $I_D=250\mu A$	600	--	--	V
		125 °C, $V_{GS}=0V$ , $I_D=250\mu A$	600	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	25 °C, $V_{DS}=600V$ , $V_{GS}=0V$	--	--	10	$\mu A$
		125 °C, $V_{DS}=600V$ , $V_{GS}=0V$	--	--	50	$\mu A$
		150 °C, $V_{DS}=600V$ , $V_{GS}=0V$	--	--	100	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V$ , $V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V$ , $I_D=5.0A$	--	0.75	1.0	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=25V$ , $V_{GS}=0V$ , $f=1.0MHZ$	--	1132	--	pF
Output Capacitance	$C_{oss}$		--	135	--	
Reverse Transfer Capacitance	$C_{rss}$		--	3.91	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V$ , $I_D=10A$ , $R_G=25\Omega$  (Note 2,3)	--	32.33	--	ns
Turn-on Rise Time	$t_r$		--	60.40	--	
Turn-off Delay Time	$t_{d(off)}$		--	58.67	--	
Turn-off Fall Time	$t_f$		--	38.67	--	
Total Gate Charge	$Q_g$	$V_{DS}=480V$ , $I_D=10A$ , $V_{GS}=10V$  (Note 2,3)	--	19.38	--	nC
Gate-Source Charge	$Q_{gs}$		--	6.26	--	
Gate-Drain Charge	$Q_{gd}$		--	6.55	--	

**Source-Drain Diode Ratings And Characteristics**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse p-n Junction Diode in the MOSFET	--	--	10	A
Pulsed Source Current	$I_{SM}$		--	--	40	
Diode Forward Voltage	$V_{SD}$	$I_S=10A$ , $V_{GS}=0V$	--	--	1.3	V
Reverse Recovery Time	$T_{rr}$	$I_S=10A$ , $V_{GS}=0V$ , $di_F/dt=100A/\mu S$ (Note 2)	--	535.39	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	4.6	--	$\mu C$

**Notes:**

1.  $L=30mH$ ,  $I_{AS}=6.0A$ ,  $V_{DD}=150V$ ,  $R_G=25\Omega$ , starting  $T_J=25^{\circ}C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

## Typical Characteristics

Figure 1. On-Region Characteristics

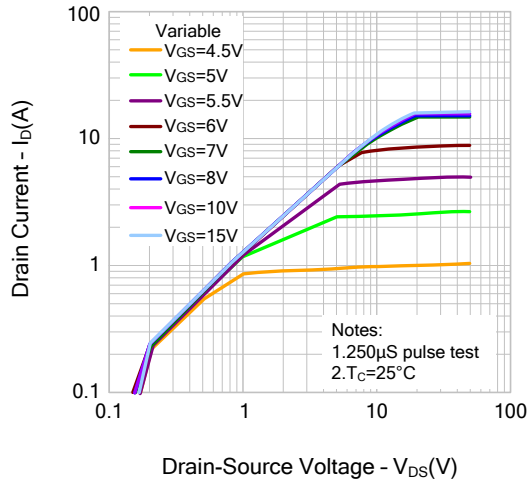


Figure 2. Transfer Characteristics

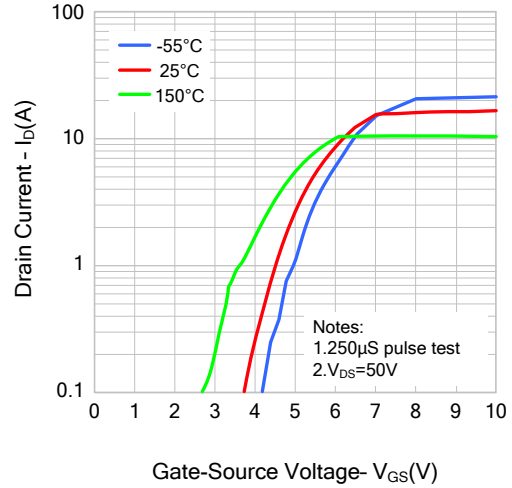


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

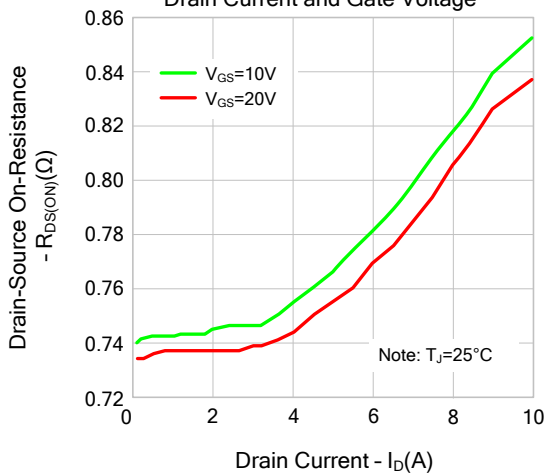


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

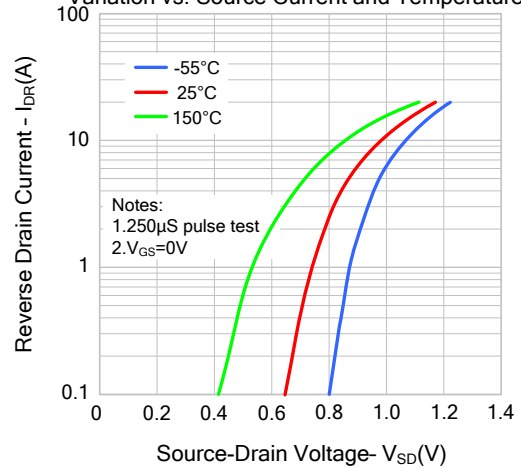


Figure 5. Capacitance Characteristics

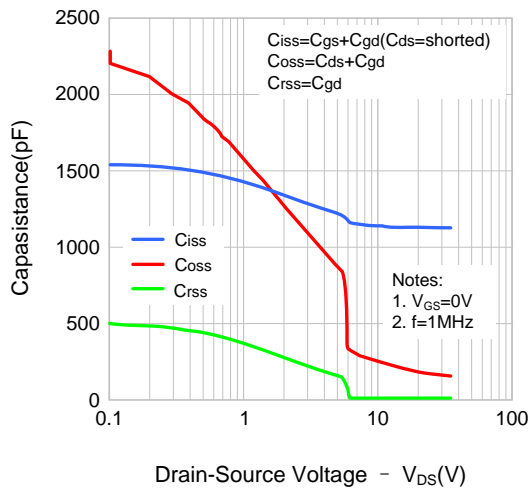
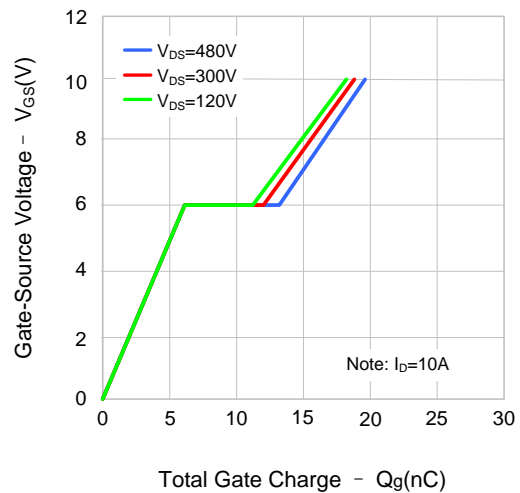
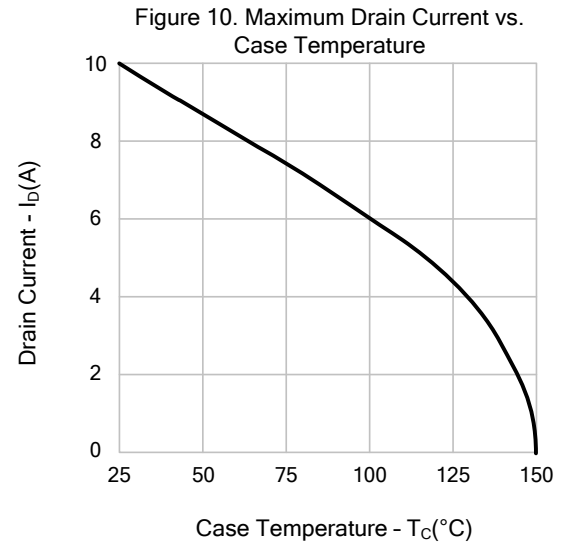
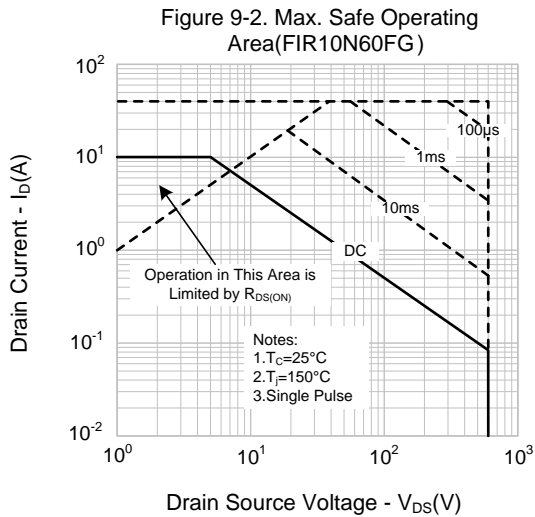
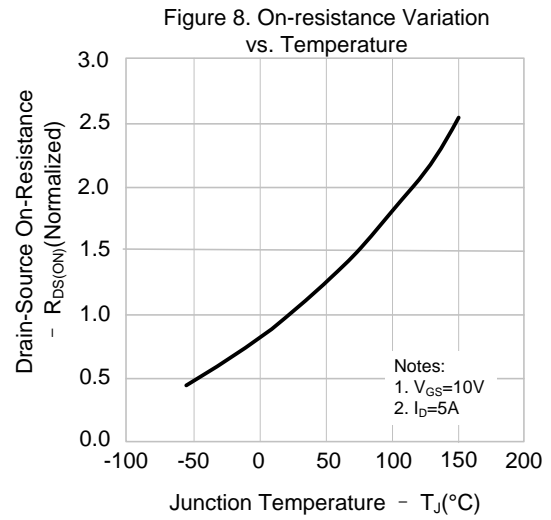
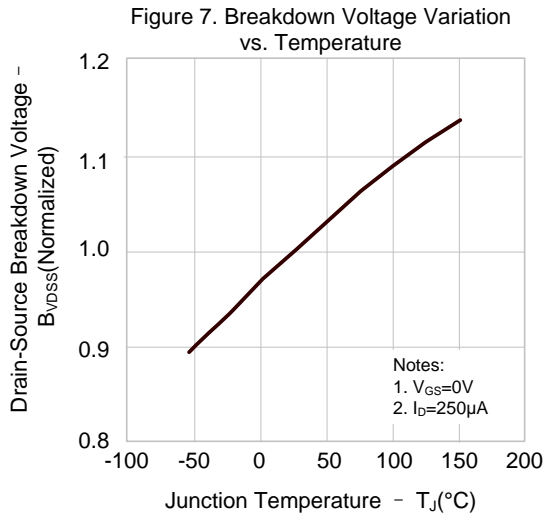


Figure 6. Gate Charge Characteristics

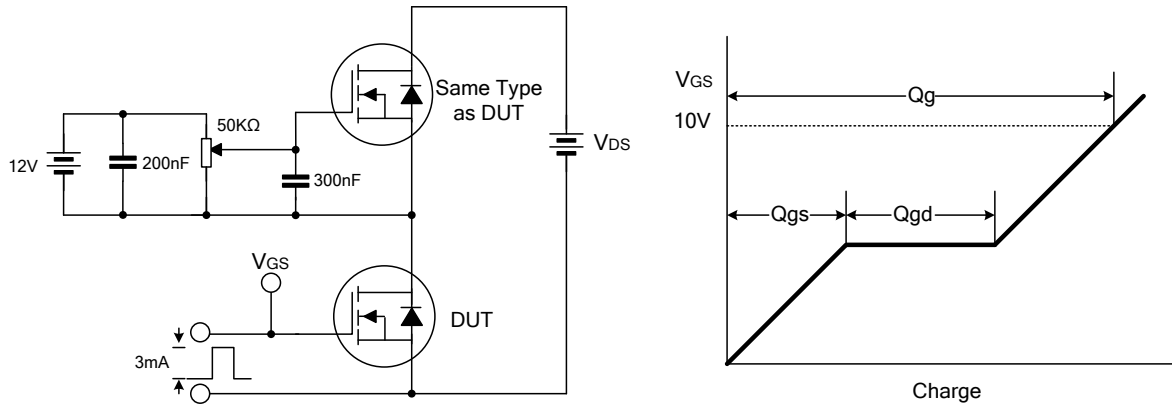


## Typical Characteristics(Continued)

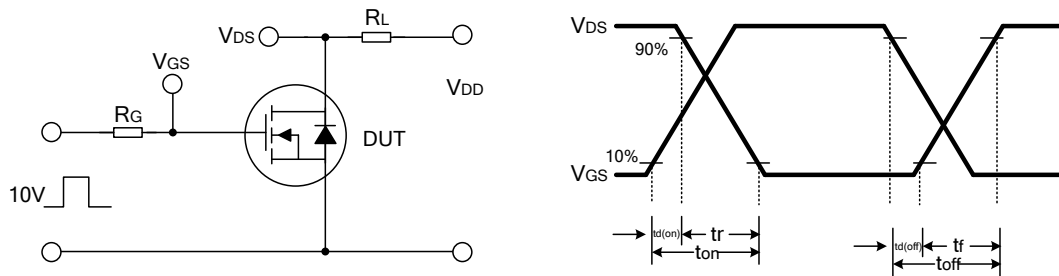


## Typical Test Circuit

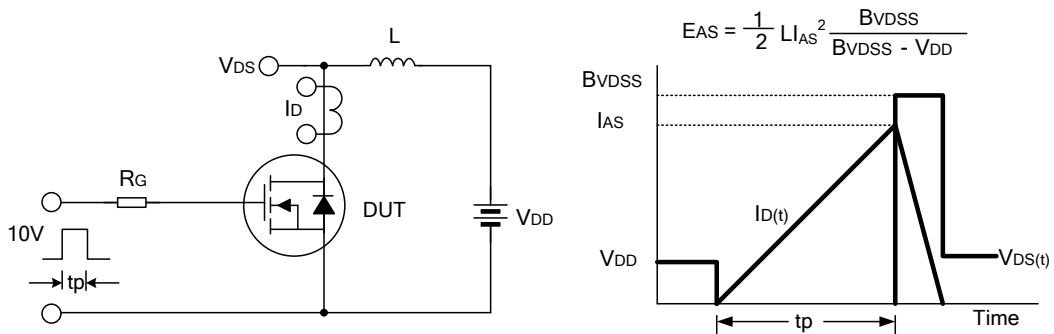
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

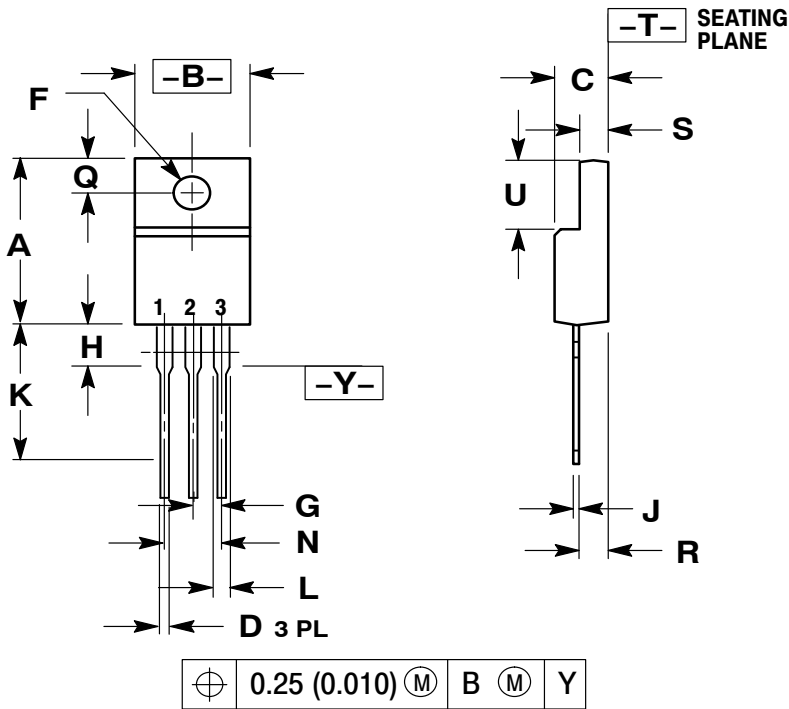


Unclamped Inductive Switching Test Circuit & Waveform



## Package Dimensions

### TO-220F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88