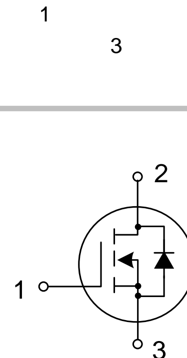
PIN Connection TO-252(D-PAK)



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FIR4N60LG is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

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- x 4A,600V,$R_{DS(on)}$ Ätyp Å=2.0 : @V_{GS}=10V
- x Low gate charge
- x Low Crss
- x Fast switching
- x Improved dv/dt capability

Marking Diagram

YAWW
FIR4N60L

Y	= Year
A	= Assembly Location
WW	= Work Week
FIR4N60L	= Specific Device Code

! " # $ %& ' unless otherwise noted; reference only(

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	4.0	A
	T_C=100°C		2.5	
Drain Current Pulsed		I_{DM}	16	A
Power Dissipation(T_C=25°C)		P_D	77	W
-Derate above 25°C			0.62	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	217	mJ
Operation Junction Temperature Range		T_J	-55 +150	°C
Storage Temperature Range		T_{stg}	-55 +150	°C

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Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R -&	1.61	℃/W
Thermal Resistance, Junction-to-Ambient	R -$	110	℃/W

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Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	25 ℃, V_{GS}=0V, I_D=250μA	6[illegible]	--	--	V
		125 ℃, V_{GS}=0V, I_D=250μA	6[illegible]0	[illegible]	--	V
Drain-Source Leakage Current	I_{DSS}	25 ℃, V_{DS}=800V, V_{GS}=0V	--	--	[illegible]10	uA
		125 ℃, V_{DS}=800V, V_{GS}=0V	--	--	[illegible]	uA
		150 ℃, V_{DS}=800V, V_{GS}=0V	--	[illegible]	[illegible]00	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	[illegible].0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, [illegible]	--	2.0	2.4	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	[illegible]00	--	pF
Output Capacitance	C_{oss}		--	57.57	--	
Reverse Transfer Capacitance	C_{rss}		[illegible]	2.59	--	
Turn-on Delay Time	$t_{[illegible]}$	V_{DD}=300V,I_D=4A, R[illegible]25Ω (Note2,3)	--	14.20	--	ns
Turn-on Rise Time	t_r		--	27.73	--	
Turn-off Delay Time	$t_{d(off)}$		--	34.67	--	
Turn-off Fall Time	[illegible]		--	28.53	--	
Total Gate Charge	Q_g	V_{DS}=48[illegible],I_D=4A, [illegible]V (Note 2,3)	--	11.88	--	nC
Gate-Source Charge	Q_{gs}		--	3.33	--	
Gate-Drain Charge	Q_{gd}		--	4.90	--	

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Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 2)	--	408	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.98	--	μC

Notes:

1. L=30mH, I_{AS}=3.45A, V_{DD}=100V, R_G=25 : , starting T_J=25 ℃;
2. Pulse Test: Pul V H Z L G W K ” V ' X W \ F \ F O H ”
3. Essentially independent of operating temperature.

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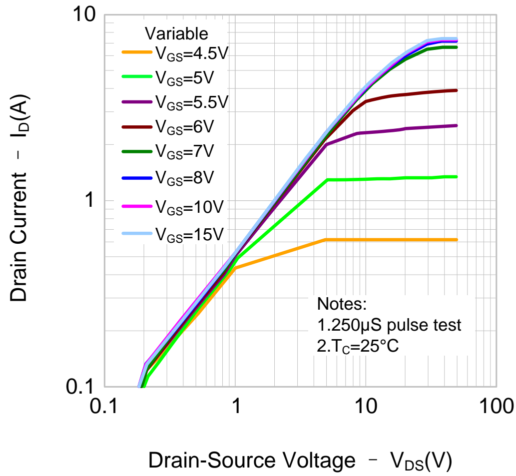

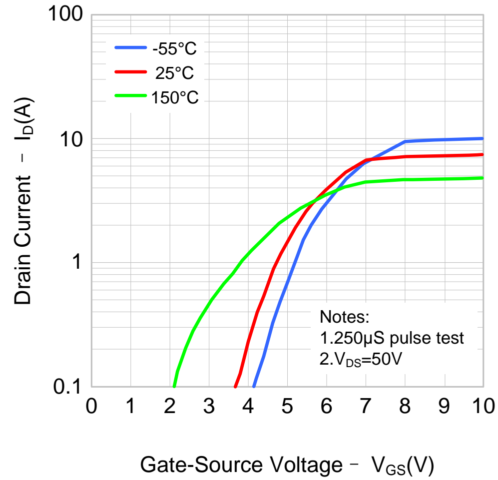

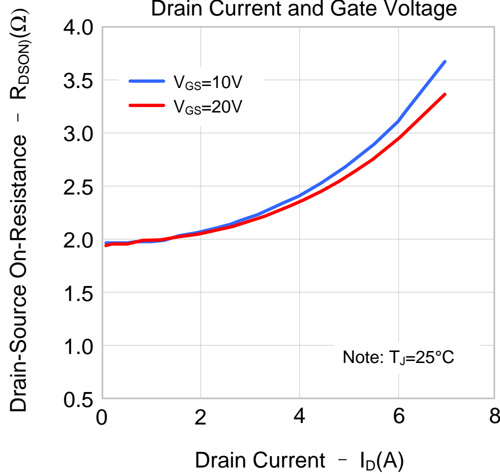

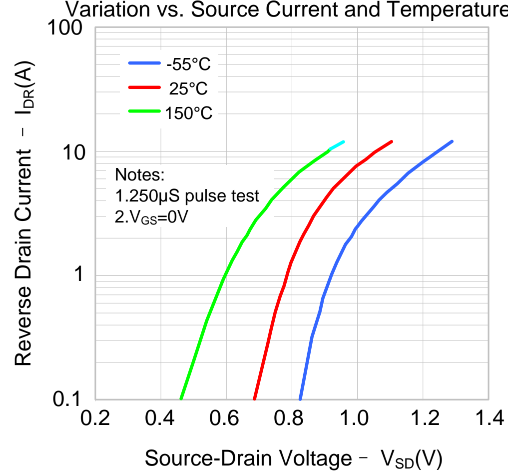

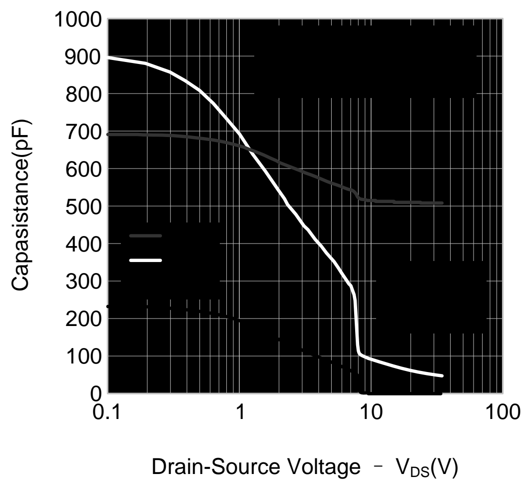

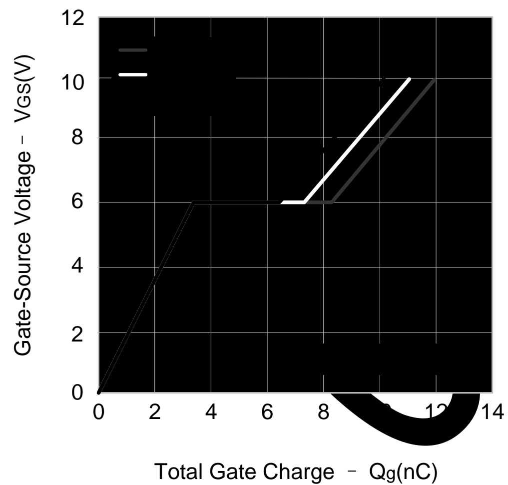

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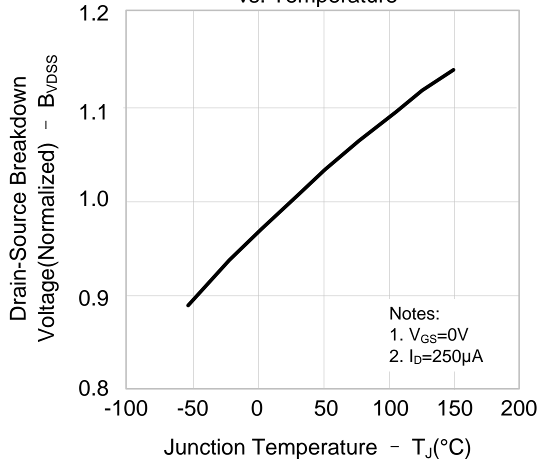

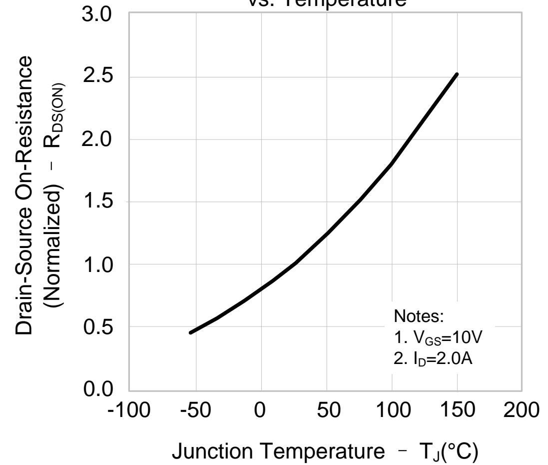

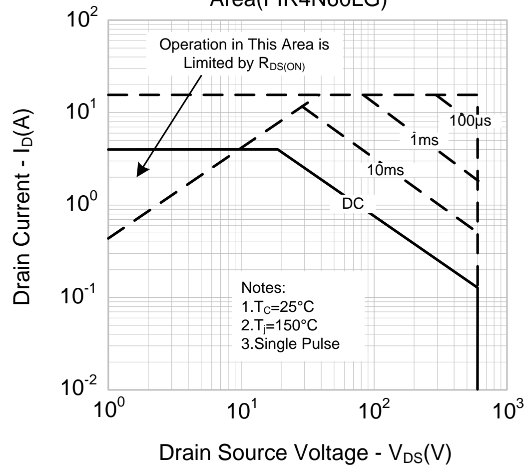

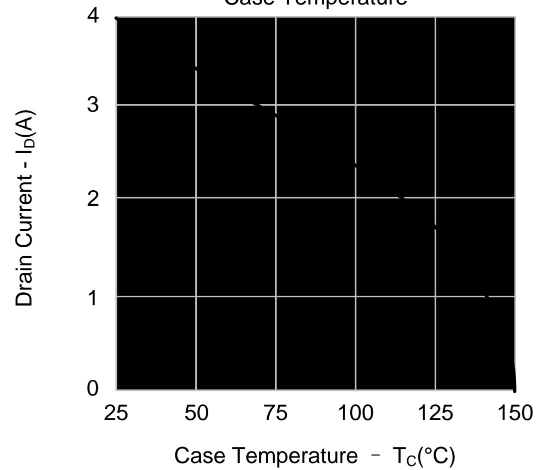

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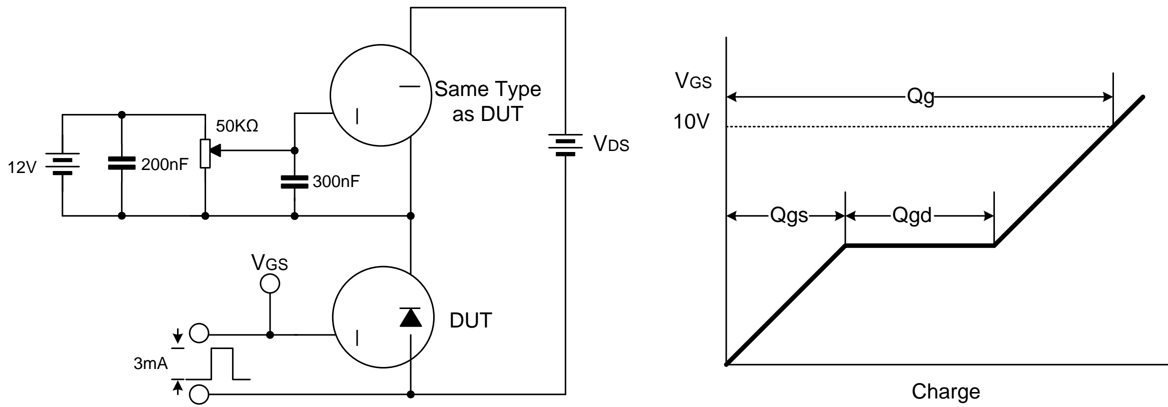
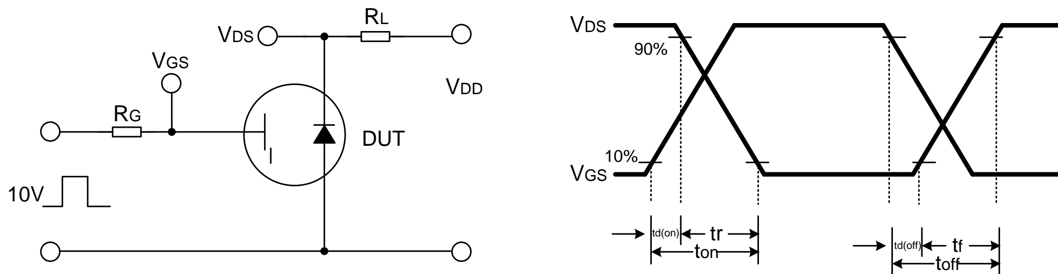
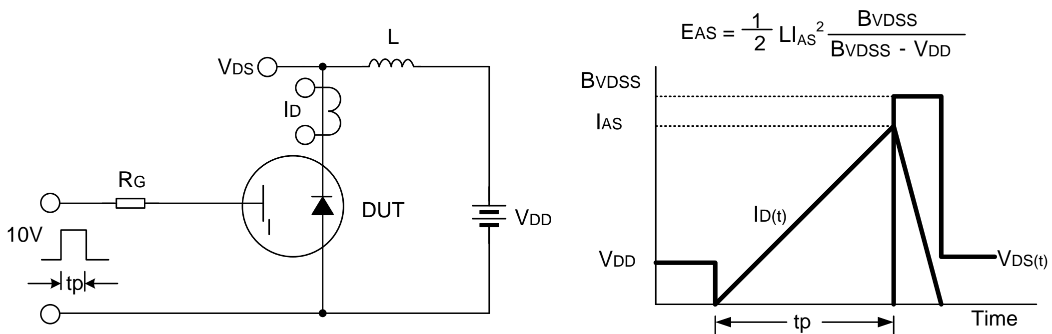
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



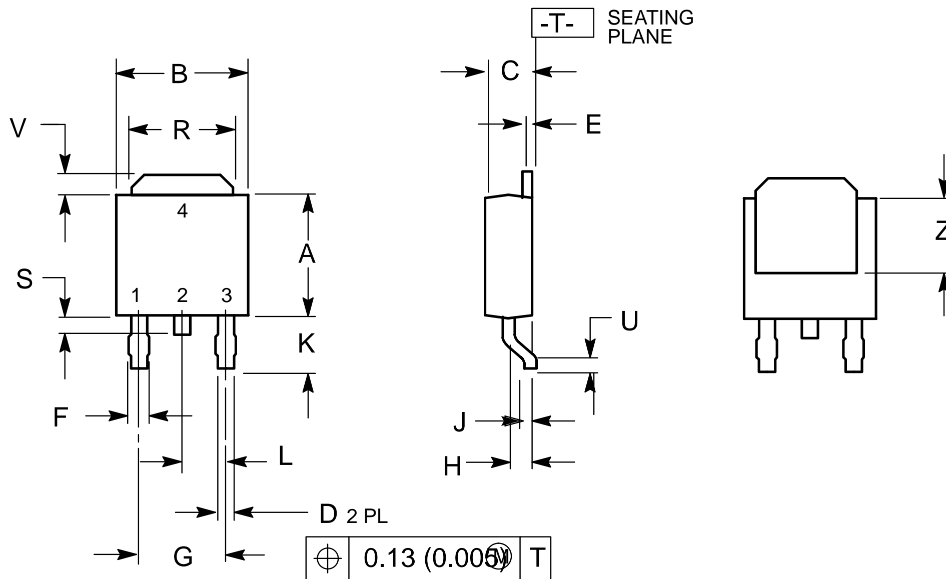
Unclamped Inductive Switching Test Circuit & Waveform



Package Dimensions

G
G

TO-252(DPAK)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---