

Description

The FIR50N055PG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

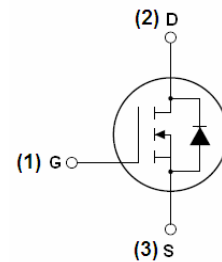
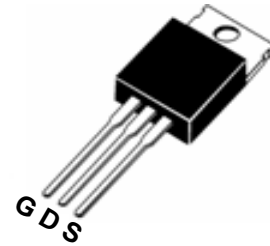
General Features

- $V_{DS} = 55V, I_D = 50A$
 $R_{DS(ON)} < 20m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

PIN Connection TO-220



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR50N055P = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR50N055P	FIR50N055PG	TO-220	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	55	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	35	A
Pulsed Drain Current	I_{DM}	150	A
Maximum Power Dissipation	P_D	80	W
Derating factor		0.53	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	115	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	1.87	$^{\circ}C/W$
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Electrical Characteristics (TA=25°C unless otherwise noted)

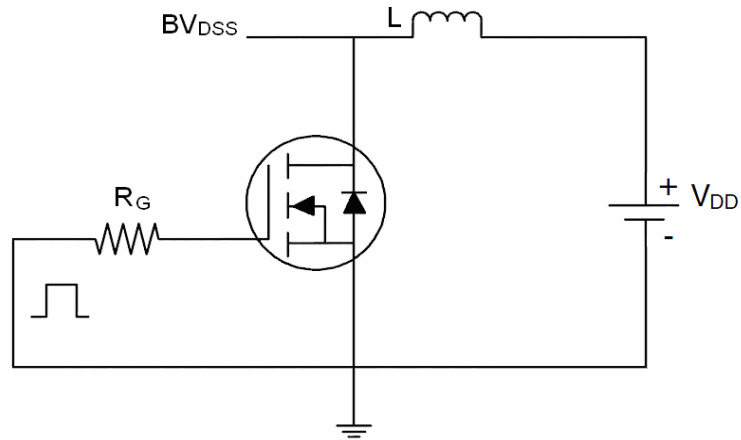
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	55	65	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	17	20	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=20A$	24	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	1200	-	PF
Output Capacitance	C_{OSS}		-	104	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	33	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	25	-	nS
Turn-on Rise Time	t_r		-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	t_f		-	6	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=50A,$ $V_{GS}=10V$	-	30		nC
Gate-Source Charge	Q_{gs}		-	10		nC
Gate-Drain Charge	Q_{gd}		-	5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=40A$	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	50	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 40A$	-	50	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note3)	-	100	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

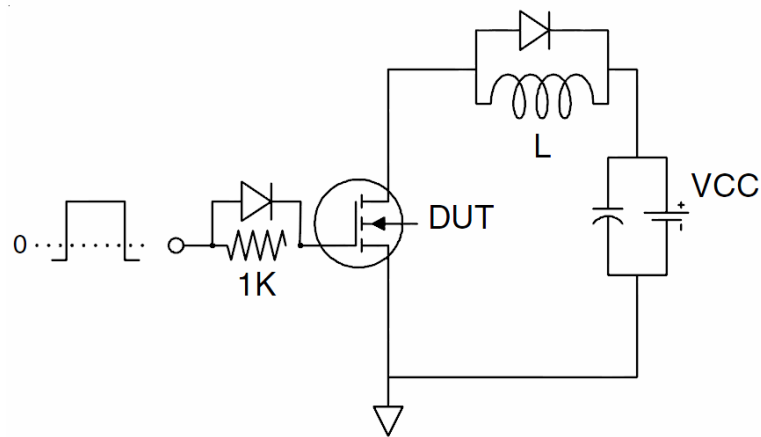
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

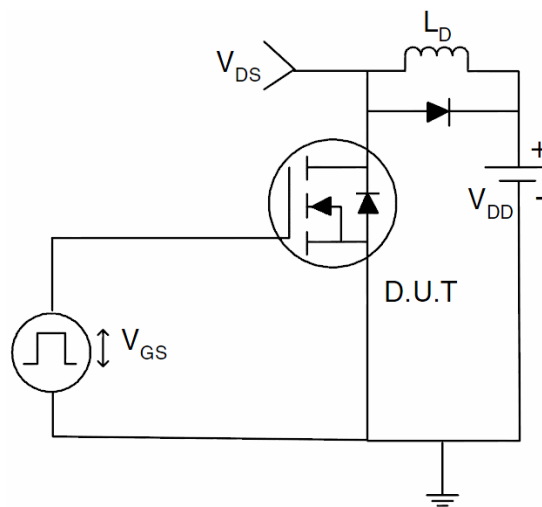
1) E_{AS} test Circuits

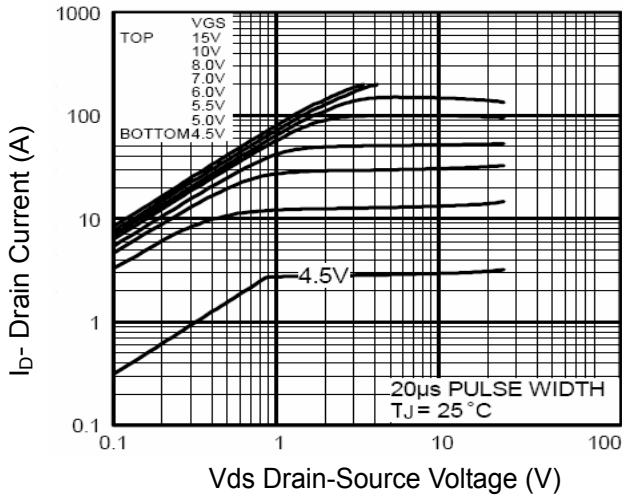
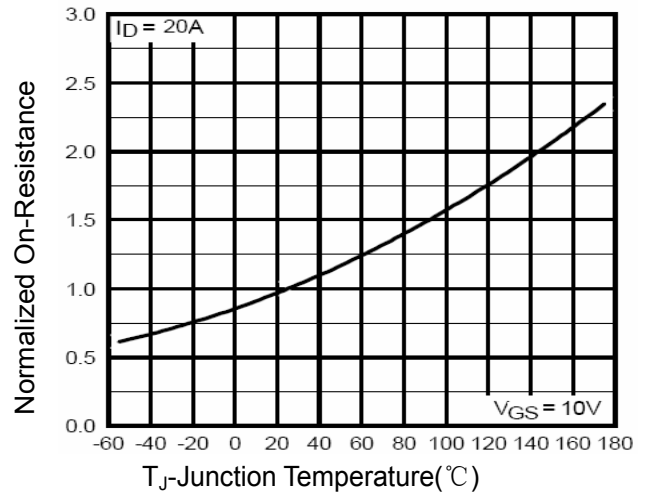
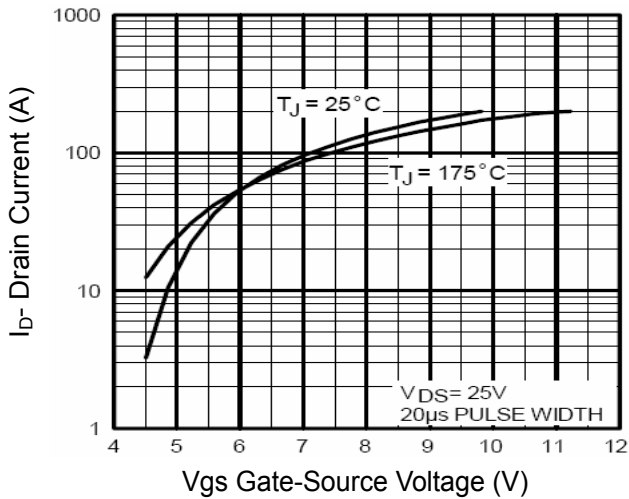
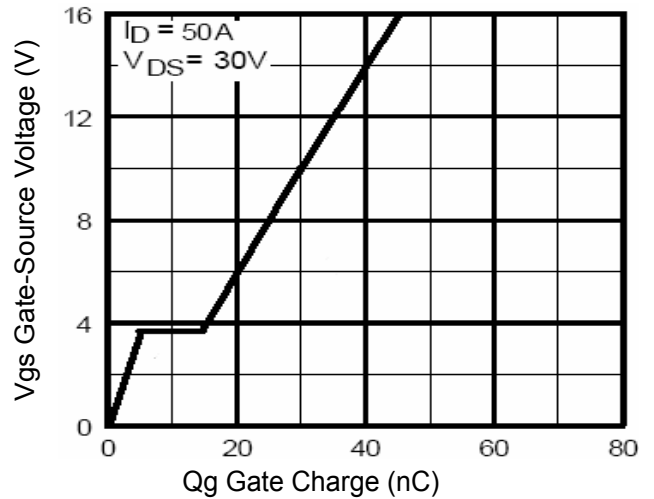
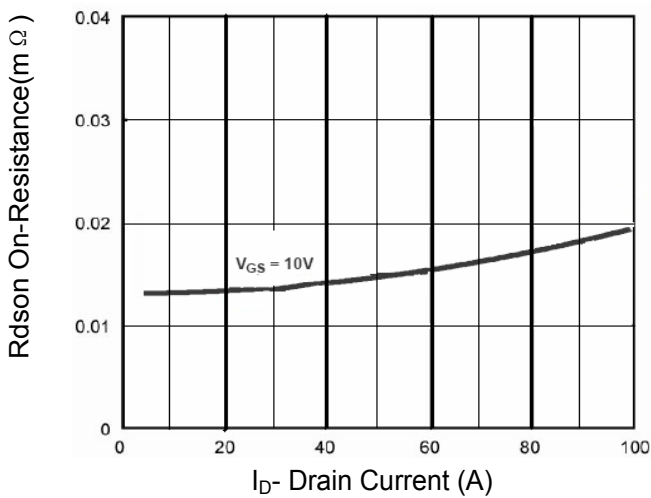
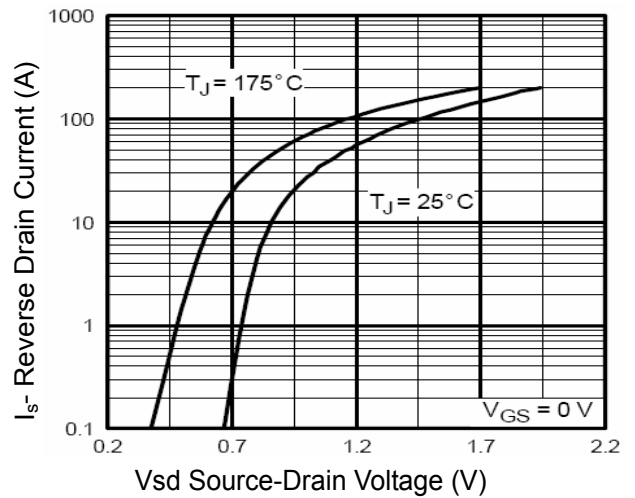


2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical And Thermal Characteristics(Curves)

Figure 1 Output Characteristics

Figure 4 Rdson-Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward

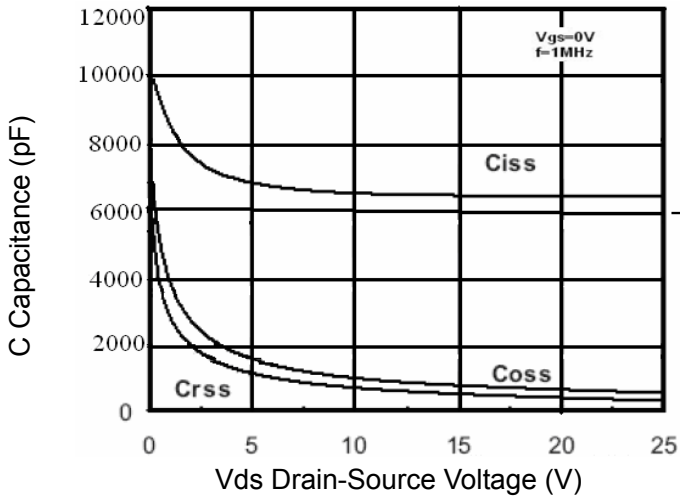


Figure 7 Capacitance vs Vds

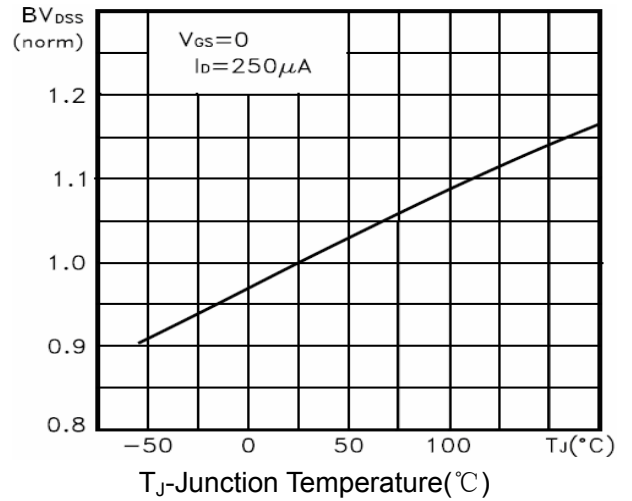


Figure 9 BV_{DSS} vs Junction Temperature

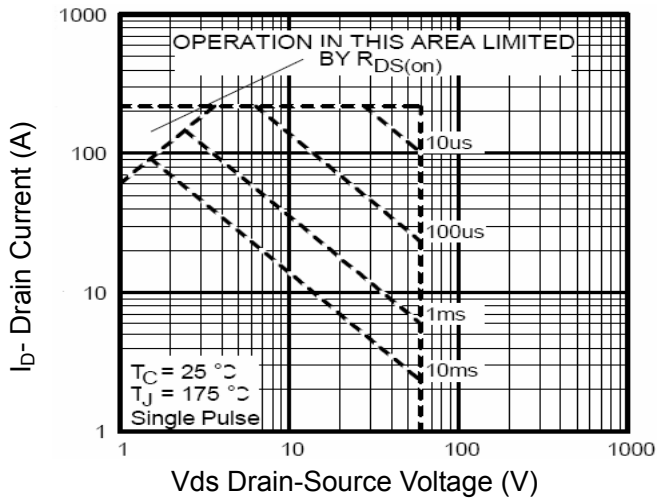


Figure 8 Safe Operation Area

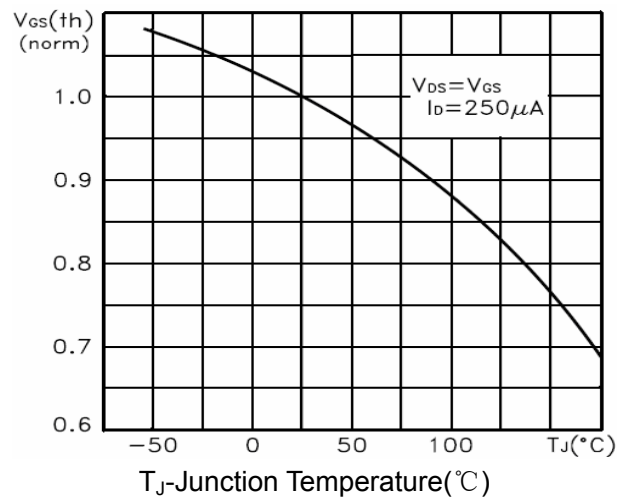


Figure 10 $V_{GS(th)}$ vs Junction Temperature

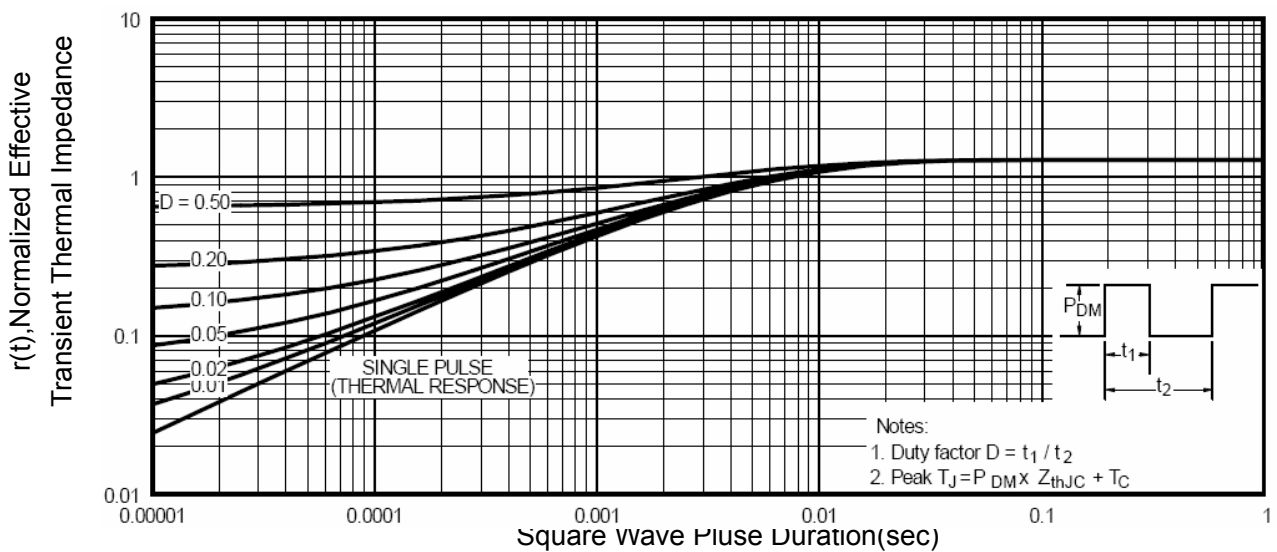
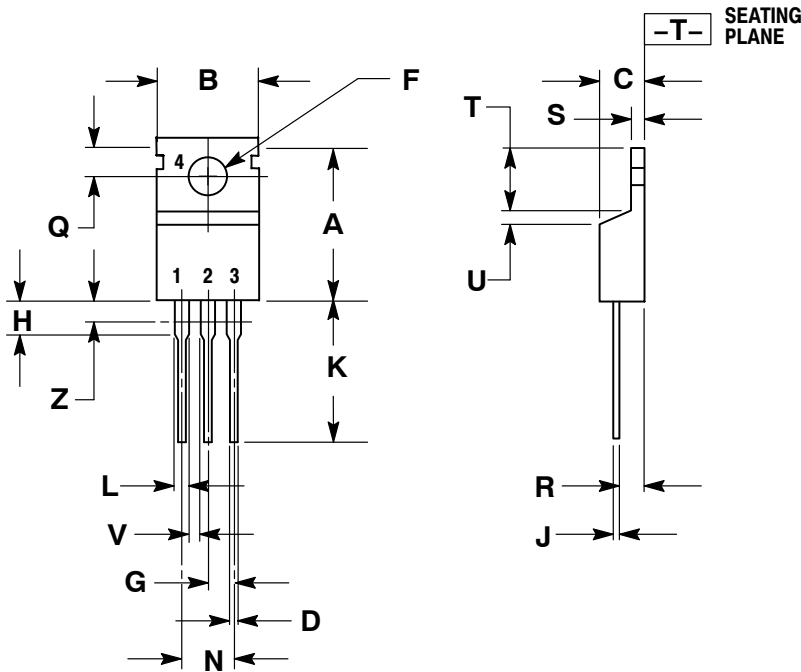


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Dimensions
TO-220

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 6:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE