

PIN Connection TO-220F

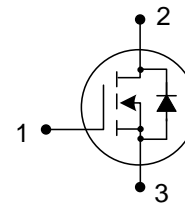
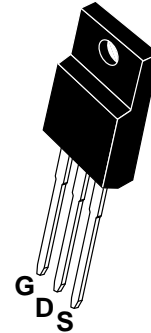
General Description

FIR6N60FG is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

Features

- 6A,600V, $R_{DS(on)}$ (typ) = 1.4 Ω @ $V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR6N60F = Specific Device Code

! " # \$ % & ' unless otherwise noted

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current	I_D	$T_C=25^\circ C$	6.0
		$T_C=100^\circ C$	3.6
Drain Current Pulsed	I_{DM}	20	A
Power Dissipation($T_C=25^\circ C$) -Derate above 25°C	P_D	85	W
		0.36	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	320	mJ
Operation Junction Temperature Range	T_J	-55 +150	°C
Storage Temperature Range	T_{stg}	-55 +150	°C

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.47	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^{\circ}C/W$

unless otherwise noted

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	25 $\text{ }^{\circ}\text{C}$, $V_{GS}=0V$, $I_D=250\mu A$	600	--	--	V
		125 $\text{ }^{\circ}\text{C}$, $V_{GS}=0V$, $I_D=250\mu A$	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	25 $\text{ }^{\circ}\text{C}$, $V_{DS}=600V$, $V_{GS}=0V$	--	--	10	μA
		125 $\text{ }^{\circ}\text{C}$, $V_{DS}=600V$, $V_{GS}=0V$	--	--	50	μA
		150 $\text{ }^{\circ}\text{C}$, $V_{DS}=600V$, $V_{GS}=0V$	--	--	100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V$, $V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2.0	3.1	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V$, $I_D=3.0A$	--	1.4	1.6	Ω
Input Capacitance	C_{iss}	$V_{DS}=25V$, $V_{GS}=0V$, $f=1.0\text{MHZ}$	--	510	--	pF
Output Capacitance	C_{oss}		--	65	--	
Reverse Transfer Capacitance	C_{rss}		--	17	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V$, $I_D=6.0A$, $R_G=25\Omega$ (Note 2,3)	--	17	--	ns
Turn-on Rise Time	t_r		--	50	--	
Turn-off Delay Time	$t_{d(off)}$		--	50	--	
Turn-off Fall Time	t_f		--	48	--	
Total Gate Charge	Q_g	$V_{DS}=480V$, $I_D=6.0A$, $V_{GS}=10V$ (Note 2,3)	--	22	--	nC
Gate-Source Charge	Q_{gs}		--	2.6	--	
Gate-Drain Charge	Q_{gd}		--	12	--	

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	6.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	$I_S=6.0A$, $V_{GS}=0V$	--	--	1.5	V
Reverse Recovery Time	T_{rr}	$I_S=6.0A$, $V_{GS}=0V$, $di_F/dt=100A/\mu S$	--	300	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.1	--	μC

Notes:

- $L=30\text{mH}$, $I_{AS}=5.16A$, $V_{DD}=159V$, $R_G=25\Omega$; starting $T_J=25\text{ }^{\circ}\text{C}$;
- Pulse Test: P X O V H Z L G W K " V ' X W \ F \ F O H "
- Essentially independent of operating temperature.

*0 '))

Figure 1. On-Region Characteristics

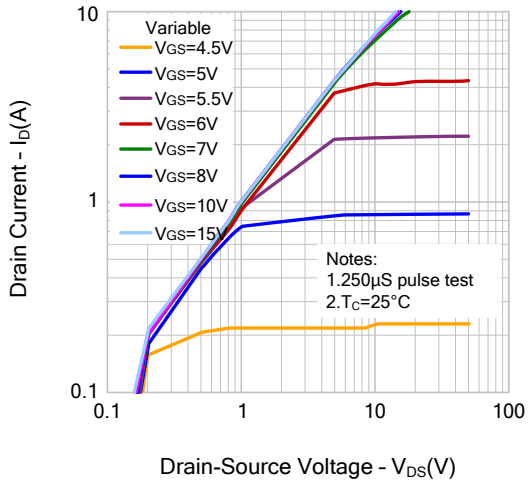


Figure 2. Transfer Characteristics

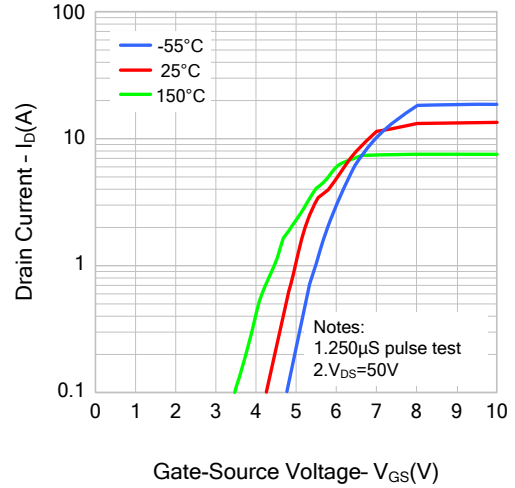


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

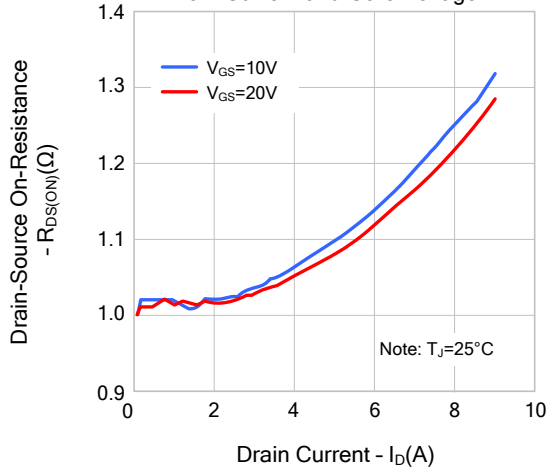


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

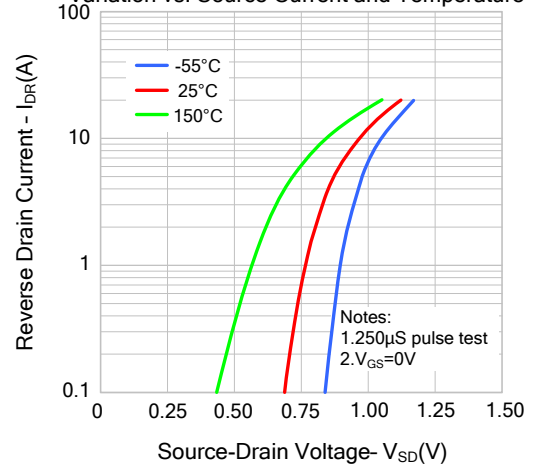


Figure 5. Capacitance Characteristics

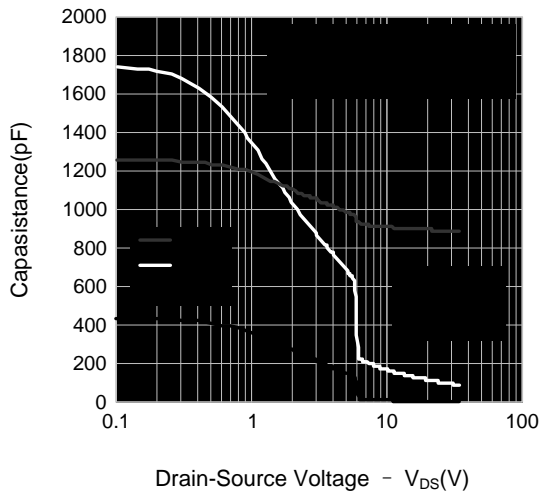
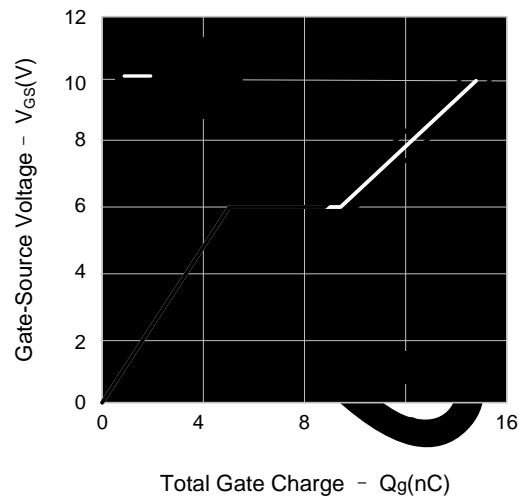


Figure 6. Gate Charge Characteristics



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Figure 7. Breakdown Voltage Variation vs. Temperature

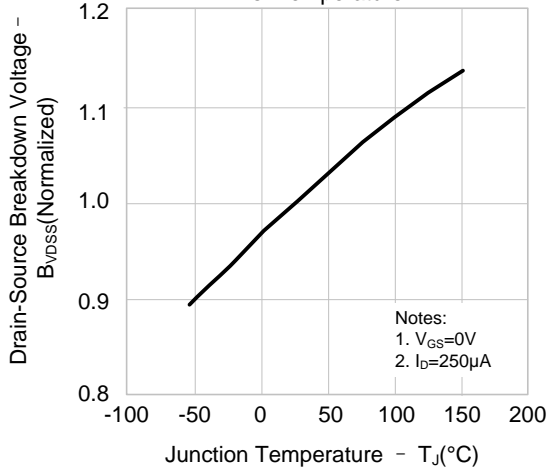


Figure 8. On-resistance Variation vs. Temperature

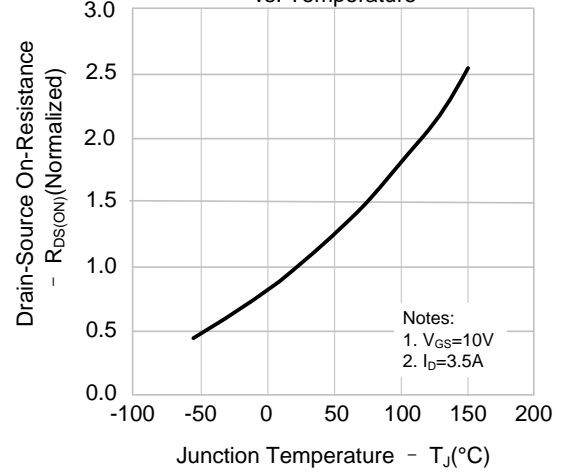


Figure 9. Max. Safe Operating Area(FIR6N60FG)

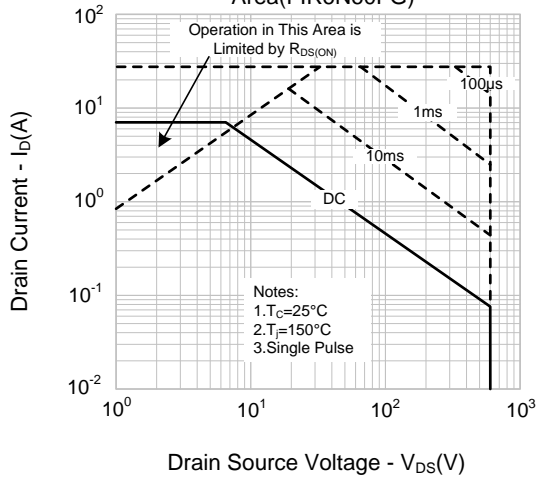
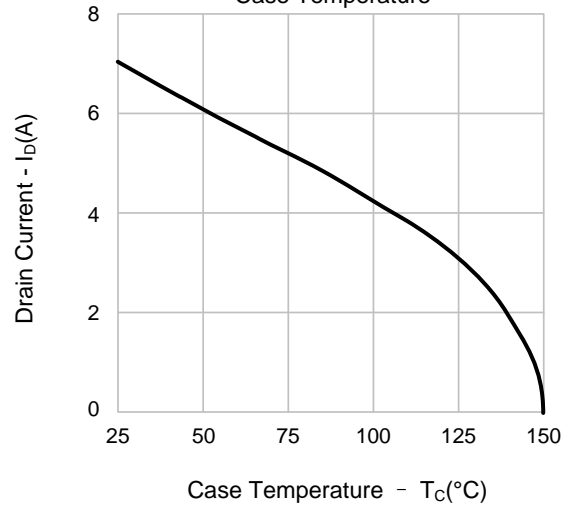
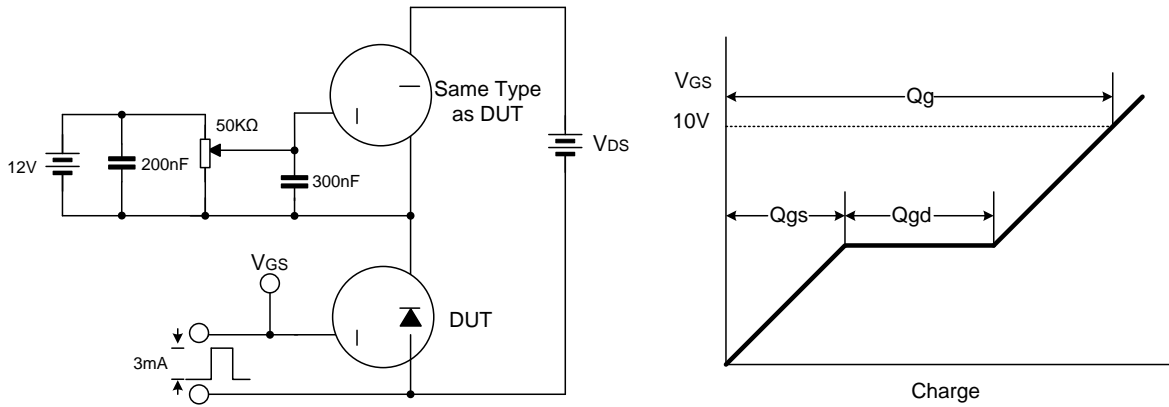


Figure 10. Maximum Drain Current vs. Case Temperature

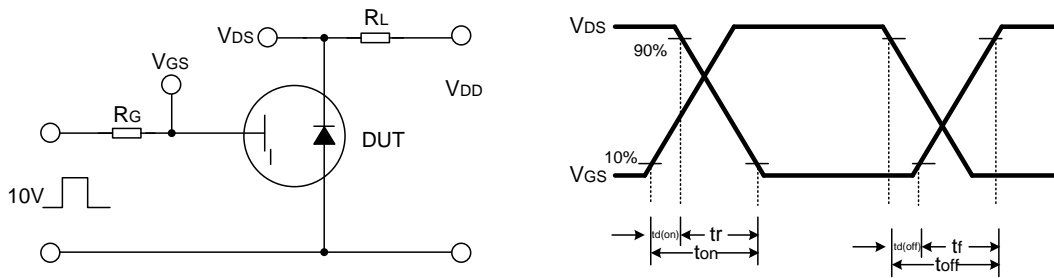


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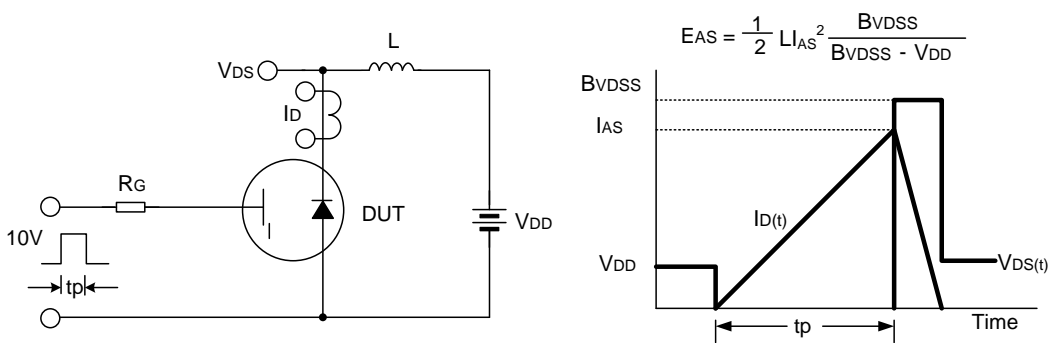
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



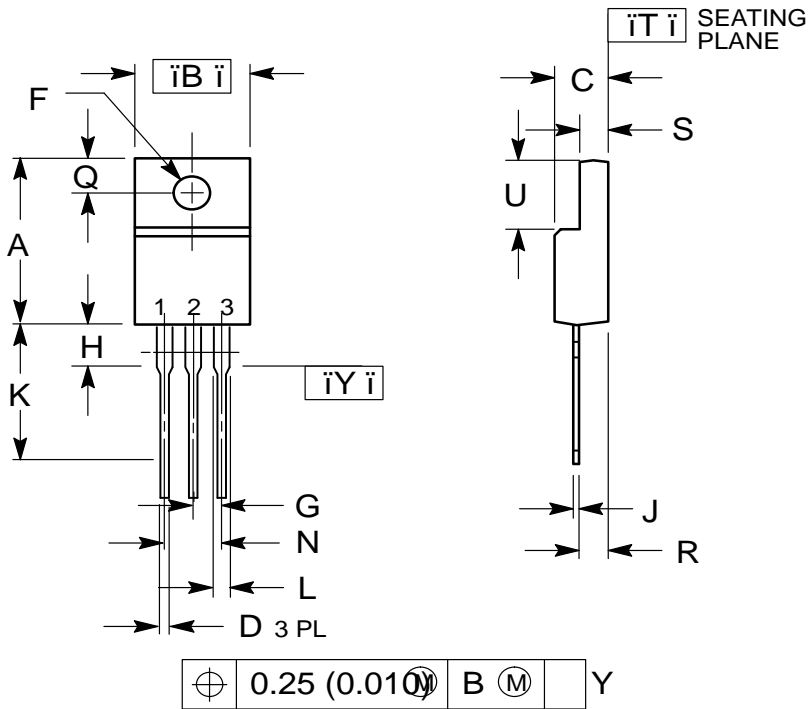
Unclamped Inductive Switching Test Circuit & Waveform



Package Dimensions

G
G

TO-220F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88