

## 600 nA, Rail-to-Rail Input/Output Op Amps

### Features

- Low Quiescent Current: 600 nA/Amplifier (typ)
- Rail-to-Rail Input:  $-0.3\text{ V}$  to  $V_{DD}+0.3\text{ V}$  (max)
- Rail-to-Rail Output:  
 $V_{SS}+10\text{ mV}$  to  $V_{DD}-10\text{ mV}$  (max)
- Gain Bandwidth Product: 14 kHz (typ)
- Wide Supply Voltage Range: 1.4 V to 5.5 V (max)
- Unity Gain Stable
- Available in Single, Dual and Quad
- Chip Select ( $\overline{\text{CS}}$ ) with MCP6043
- 5-lead SOT-23 package (MCP6041 only)

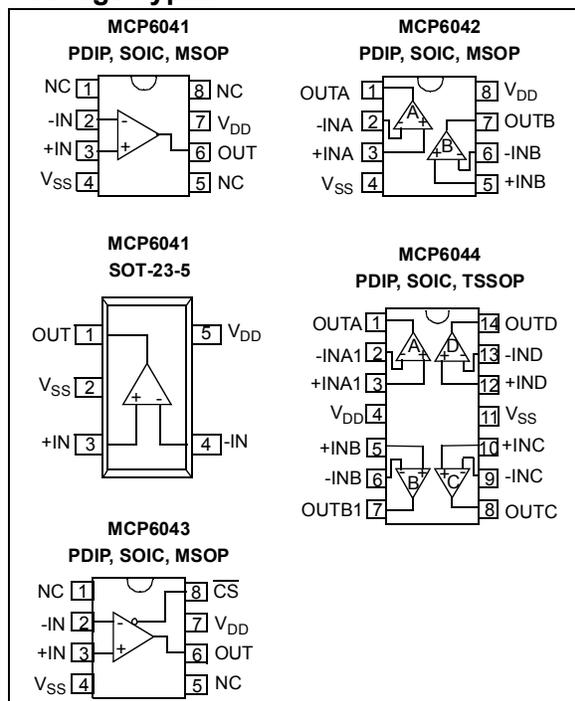
### Applications

- Toll Booth Tags
- Wearable Products
- Temperature Measurement
- Battery Powered

### Available Tools

- Spice macro models (at [www.microchip.com](http://www.microchip.com))
- FilterLab<sup>®</sup> Software (at [www.microchip.com](http://www.microchip.com))

### Package Types



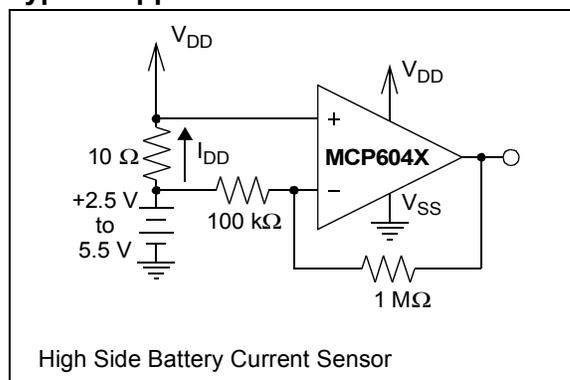
### Description

The MCP6041/2/3/4 family of operational amplifiers from Microchip Technology, Inc. operate with a single supply voltage as low as 1.4 V, while drawing less than 1  $\mu\text{A}$  (max) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

The MCP6041/2/3/4 amplifiers have a typical gain bandwidth product of 14 kHz (typ) and are unity gain stable. These specs make these operational amplifiers appropriate for low frequency applications, such as battery current monitoring and sensor conditioning.

The MCP6041/2/3/4 family operational amplifiers are offered in single (MCP6041), single with a Chip Select ( $\overline{\text{CS}}$ ) feature (MCP6043), dual (MCP6042) and quad (MCP6044) configurations. The MCP6041 device is available in the 5-lead SOT-23 package.

### Typical Application



# MCP6041/2/3/4

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

$V_{DD} - V_{SS}$ .....	7.0 V
All inputs and outputs.....	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
Difference Input voltage .....	$ V_{DD} - V_{SS} $
Output Short Circuit Current .....	continuous
Current at Input Pins .....	$\pm 2$ mA
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage temperature .....	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Ambient temp. with power applied .....	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
ESD protection on all pins (HBM).....	$\geq 4$ kV

\*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

Name	Function
+IN/+INA/+INB/+INC/+IND	Non-inverting Inputs
-IN/-INA/-INB/-INC/-IND	Inverting Inputs
$V_{DD}$	Positive Power Supply
$V_{SS}$	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Outputs
$\overline{\text{CS}}$	Chip Select
NC	No internal connection to IC

## MCP6041/2/3/4 DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{DD} = +1.4$ V to $+5.5$ V, $V_{SS} = \text{GND}$ , $T_A = 25^{\circ}\text{C}$ , $V_{CM} = V_{DD}/2$ , $R_L = 1$ M $\Omega$ to $V_{DD}/2$ , and $V_{OUT} \sim V_{DD}/2$							
Parameters	Sym	Min	Typ	Max	Units	Conditions	
<b>Input Offset:</b>							
Input Offset Voltage	$V_{OS}$	-3.0	—	+3.0	mV	$V_{CM} = V_{SS}$	
Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	$\pm 1.5$	—	$\mu\text{V}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	
Power Supply Rejection	PSRR	70	85	—	dB		
<b>Input Bias Current and Impedance:</b>							
Input Bias Current	$I_B$	—	1.0	—	$\mu\text{A}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}$	
Input Bias Current Over Temperature	$I_B$	—	—	100	$\mu\text{A}$		
Input Offset Current	$I_{OS}$	—	1.0	—	$\mu\text{A}$		
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  6$	—	$\Omega  \text{pF}$		
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  6$	—	$\Omega  \text{pF}$		
<b>Common Mode:</b>							
Common-Mode Input Range	VCMR	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	$V_{DD} = 5$ V, $V_{CM} = -0.3$ V to $5.3$ V	
Common-Mode Rejection Ratio	CMRR	62	80	—	dB		
		60	75	—	dB		$V_{DD} = 5$ V, $V_{CM} = 2.5$ V to $5.3$ V
		60	80	—	dB		$V_{DD} = 5$ V, $V_{CM} = -0.3$ V to $2.5$ V
<b>Open Loop Gain:</b>							
DC Open Loop Gain (large signal)	$A_{OL}$	95	115	—	dB	$R_L = 50$ k $\Omega$ to $V_{DD}/2$ , $100$ mV $< V_{OUT} < (V_{DD} - 100$ mV)	
<b>Output:</b>							
Maximum Output Voltage Swing	$V_{OL}, V_{OH}$	$V_{SS} + 10$	—	$V_{DD} - 10$	mV	$R_L = 50$ k $\Omega$ to $V_{DD}/2$	
Linear Region Output Voltage Swing	$V_{OVR}$	$V_{SS} + 100$	—	$V_{DD} - 100$	mV	$R_L = 50$ k $\Omega$ to $V_{DD}/2$ , $A_{OL} \geq 95$ dB	
Output Short Circuit Current	$I_O$	—	21	—	mA	$V_{OUT} = 2.5$ V, $V_{DD} = 5$ V	
<b>Power Supply:</b>							
Supply Voltage	$V_{DD}$	1.4	—	5.5	V	$I_O = 0$	
Quiescent Current per amplifier	$I_Q$	0.3	0.6	1.0	$\mu\text{A}$		

## MCP6041/2/3/4 AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$

Parameters	Sym	Min	Typ	Max	Units	Conditions
Gain Bandwidth Product	GBWP	—	14	—	kHz	
Slew Rate	SR	—	3.0	—	V/ms	
Phase Margin	PM	—	65	—	°	G = +1
Input Voltage Noise	$E_n$	—	5.0	—	$\mu\text{Vp-p}$	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	$e_n$	—	170	—	$\text{nV}/\sqrt{\text{Hz}}$	f = 1 kHz
Input Current Noise Density	$i_n$	—	0.6	—	$\text{fA}/\sqrt{\text{Hz}}$	f = 1 kHz

## SPECIFICATIONS FOR MCP6043 CHIP SELECT FEATURE

**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for  $V_{DD} = +1.4\text{ V}$  to  $+5.5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>CS Low Specifications:</b>						
$\overline{\text{CS}}$ Logic Threshold, Low	$V_{IL}$	$V_{SS}$	—	$V_{SS} + 0.3$	V	For entire $V_{DD}$ range
$\overline{\text{CS}}$ Input Current, Low	$I_{CSL}$	—	5.0	—	pA	$\overline{\text{CS}} = V_{SS}$
<b>CS High Specifications:</b>						
$\overline{\text{CS}}$ Logic Threshold, High	$V_{IH}$	$V_{DD} - 0.3$	—	$V_{DD}$	V	For entire $V_{DD}$ range
$\overline{\text{CS}}$ Input Current, High	$I_{CSH}$	—	5.0	—	pA	$\overline{\text{CS}} = V_{DD}$
$\overline{\text{CS}}$ Input High, GND Current	$I_Q$	—	20	—	pA	$\overline{\text{CS}} = V_{DD}$
Amplifier Output Leakage, $\overline{\text{CS}}$ High	—	—	20	—	pA	$\overline{\text{CS}} = V_{DD}$
<b>Dynamic Specifications:</b>						
$\overline{\text{CS}}$ Low to Amplifier Output High Turn-on Time	$t_{ON}$	—	2.0	50	ms	$\overline{\text{CS}}$ low = $V_{SS} + 0.3\text{ V}$ , G = +1 V/V, $V_{OUT} = 0.9 V_{DD}/2$
$\overline{\text{CS}}$ High to Amplifier Output High Z	$t_{OFF}$	—	10	—	$\mu\text{s}$	$\overline{\text{CS}}$ high = $V_{DD} - 0.3\text{ V}$ , G = +1 V/V, $V_{OUT} = 0.1 V_{DD}/2$
Hysteresis	$V_{HYST}$	—	0.6	—	V	$V_{DD} = 5\text{ V}$

## MCP6041/2/3/4 TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for  $V_{DD} = +1.4\text{ V}$  to  $+5.5\text{ V}$ ,  $V_{SS} = \text{GND}$

Parameters	Symbol	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges:</b>						
Specified Temperature Range	$T_A$	-40	—	+85	$^\circ\text{C}$	Note 1
Operating Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ\text{C}$	
<b>Thermal Package Resistances:</b>						
Thermal Resistance, 5L-SOT23	$\theta_{JA}$	—	256	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	$^\circ\text{C}/\text{W}$	

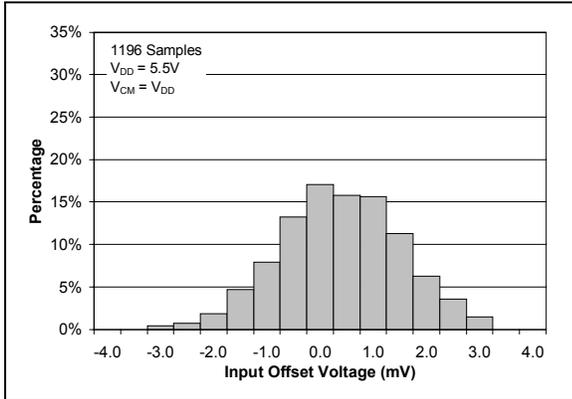
**Note 1:** The MCP6041/2/3/4 family of op amps operates over this extended range, but with reduced performance.

# MCP6041/2/3/4

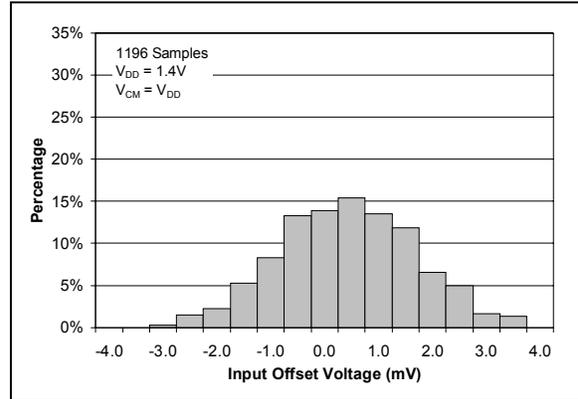
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

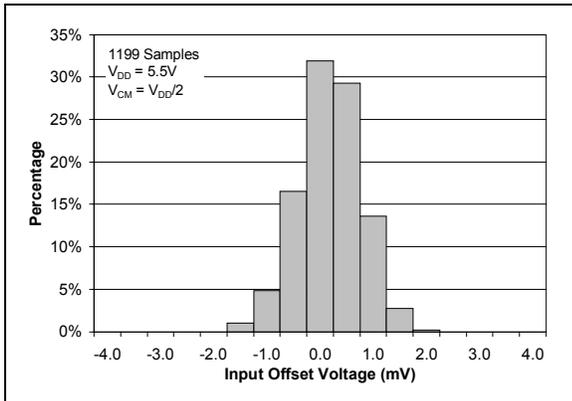
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



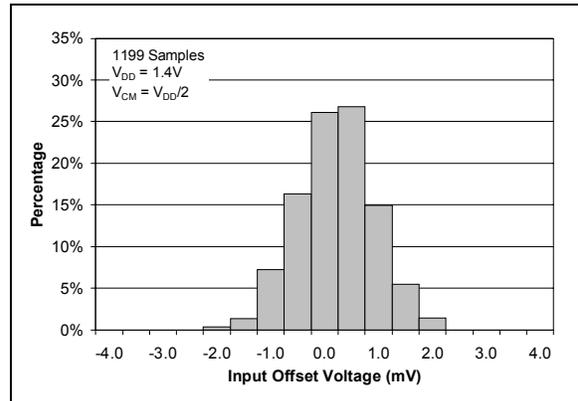
**FIGURE 2-1:** Histogram of Input Offset Voltage with  $V_{DD} = 5.5\text{ V}$ ,  $V_{CM} = V_{DD}$ .



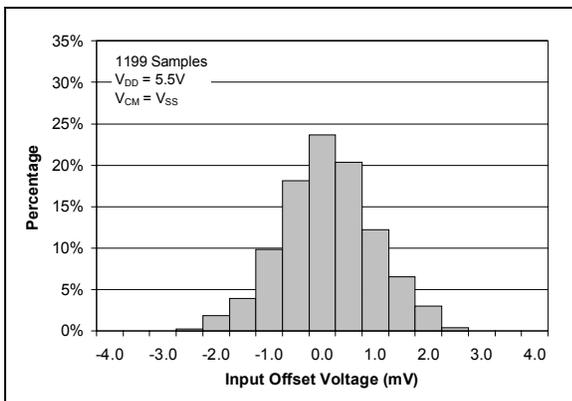
**FIGURE 2-4:** Histogram of Input Offset Voltage with  $V_{DD} = 1.4\text{ V}$ ,  $V_{CM} = V_{DD}$ .



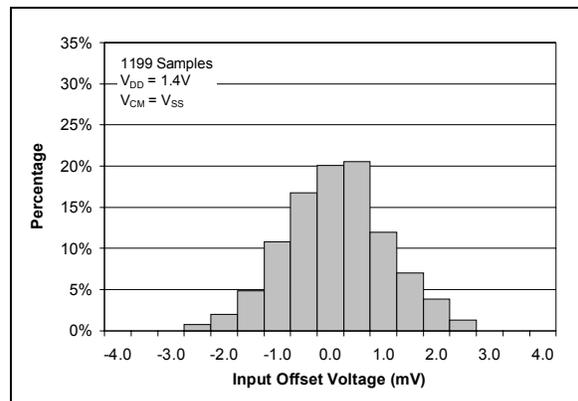
**FIGURE 2-2:** Histogram of Input Offset Voltage with  $V_{DD} = 5.5\text{ V}$ ,  $V_{CM} = V_{DD}/2$ .



**FIGURE 2-5:** Histogram of Input Offset Voltage with  $V_{DD} = 1.4\text{ V}$ ,  $V_{CM} = V_{DD}/2$ .

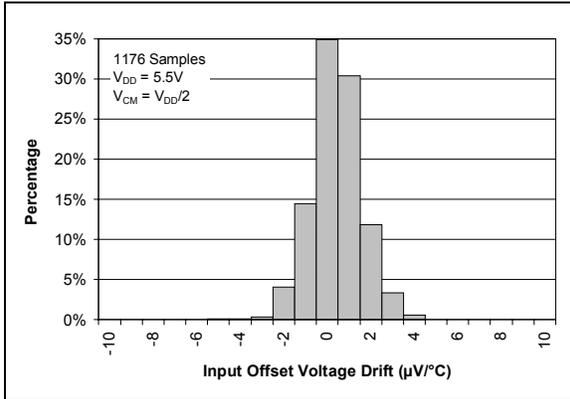


**FIGURE 2-3:** Histogram of Input Offset Voltage with  $V_{DD} = 5.5\text{ V}$ ,  $V_{CM} = V_{SS}$ .

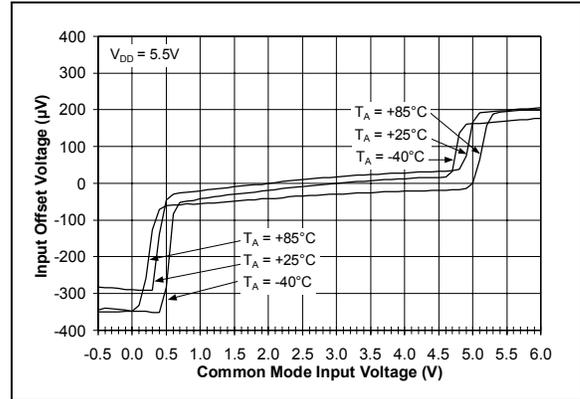


**FIGURE 2-6:** Histogram of Input Offset Voltage with  $V_{DD} = 1.4\text{ V}$ ,  $V_{CM} = V_{SS}$ .

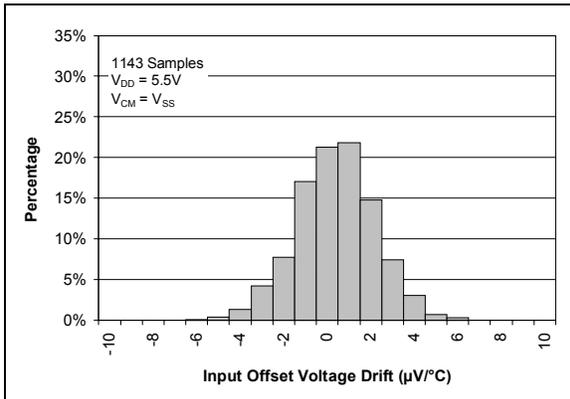
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



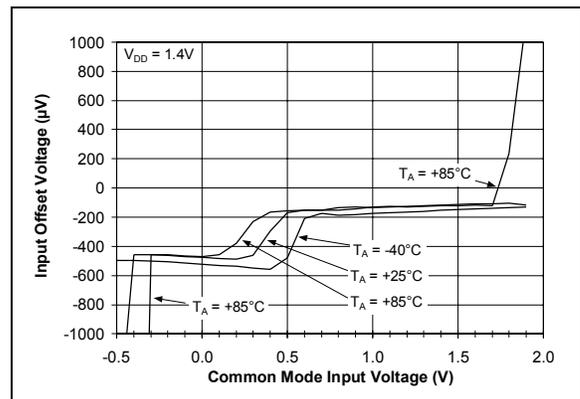
**FIGURE 2-7:** Histogram of Input Offset Voltage Drift with  $V_{DD} = 5.5\text{ V}$ ,  $V_{CM} = V_{DD}/2$ .



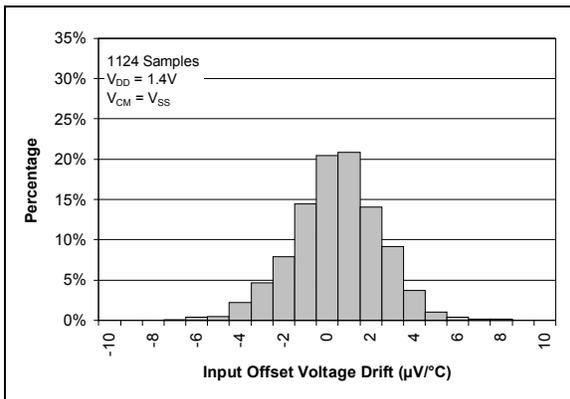
**FIGURE 2-10:** Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 5.5\text{ V}$ .



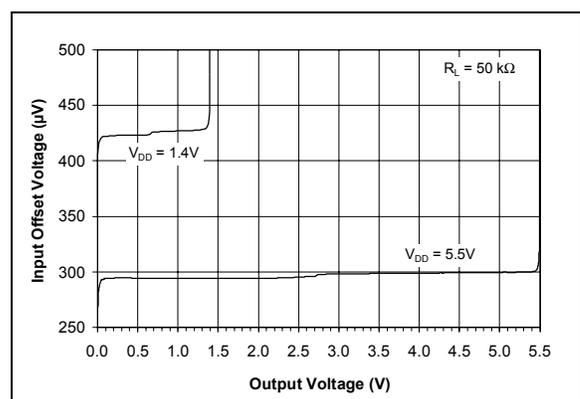
**FIGURE 2-8:** Histogram of Input Offset Voltage Drift with  $V_{DD} = 5.5\text{ V}$ ,  $V_{CM} = V_{SS}$ .



**FIGURE 2-11:** Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 1.4\text{ V}$ .



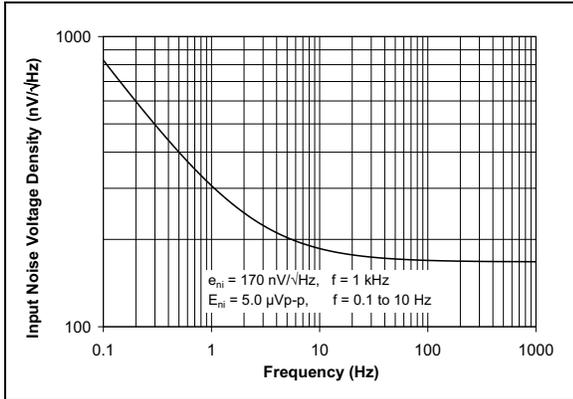
**FIGURE 2-9:** Histogram of Input Offset Voltage Drift with  $V_{DD} = 1.4\text{ V}$ ,  $V_{CM} = V_{SS}$ .



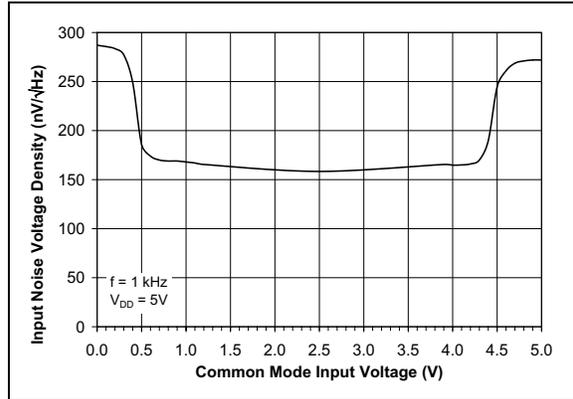
**FIGURE 2-12:** Input Offset Voltage vs. Output Voltage vs. Power Supply Voltage.

# MCP6041/2/3/4

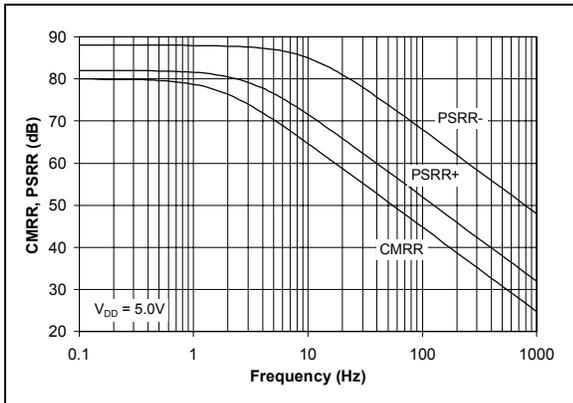
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



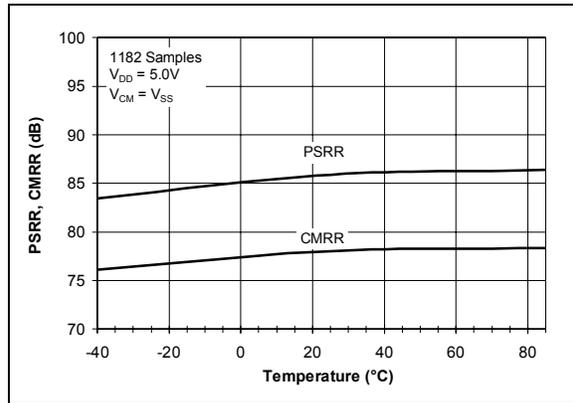
**FIGURE 2-13:** Input Noise Voltage Density vs. Frequency.



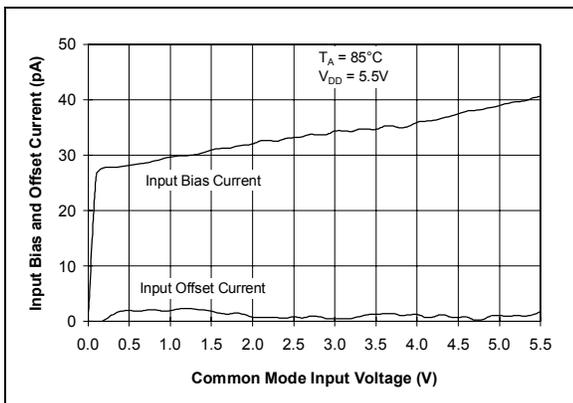
**FIGURE 2-16:** Input Noise Voltage Density vs. Common Mode Input Voltage.



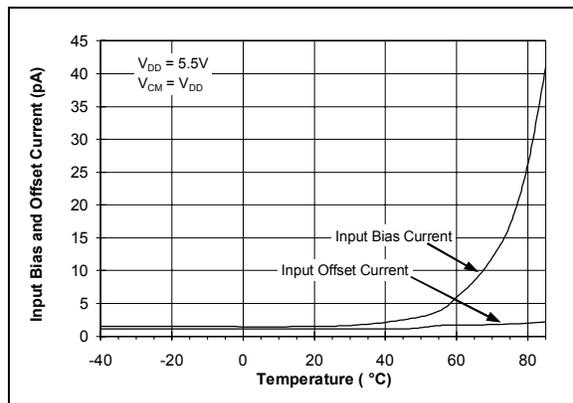
**FIGURE 2-14:** Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.



**FIGURE 2-17:** Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.

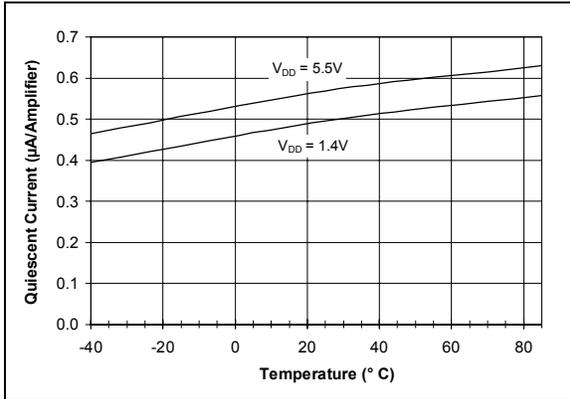


**FIGURE 2-15:** Input Bias, Offset Currents vs. Common Mode Input Voltage with Temperature =  $85^\circ\text{C}$ .

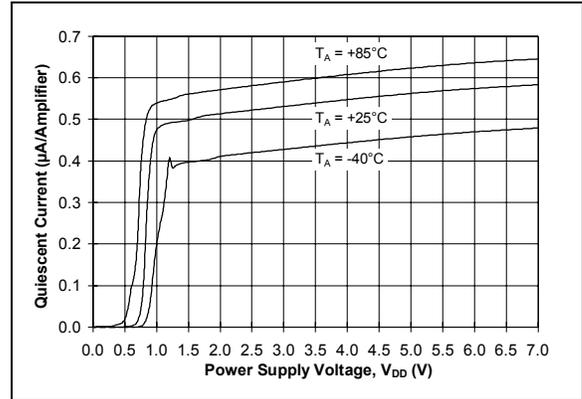


**FIGURE 2-18:** Input Bias, Offset Currents vs. Temperature.

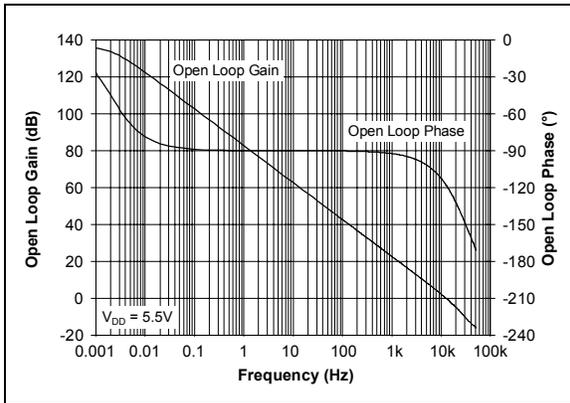
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



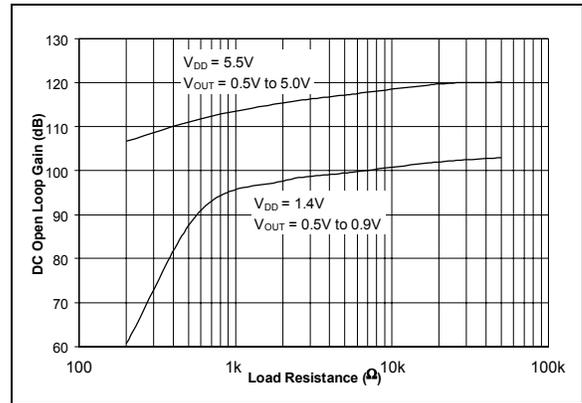
**FIGURE 2-19:** Quiescent Current vs. Temperature vs. Power Supply Voltage.



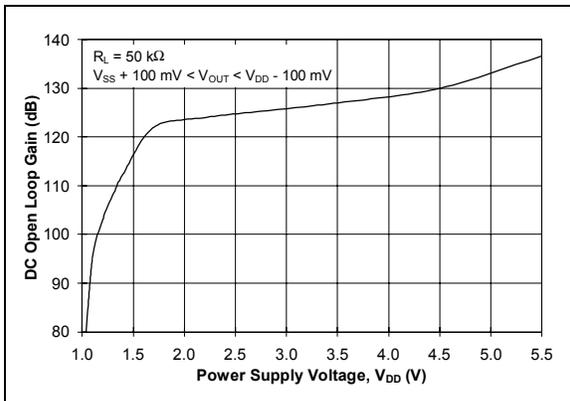
**FIGURE 2-22:** Quiescent Current vs. Power Supply Voltage vs. Temperature.



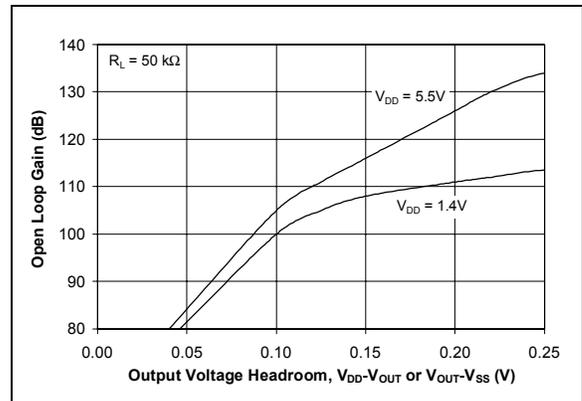
**FIGURE 2-20:** Open Loop Gain, Phase vs. Frequency with  $V_{DD} = 5.5\text{ V}$ .



**FIGURE 2-23:** Open Loop Gain vs. Load Resistance vs. Power Supply Voltage.



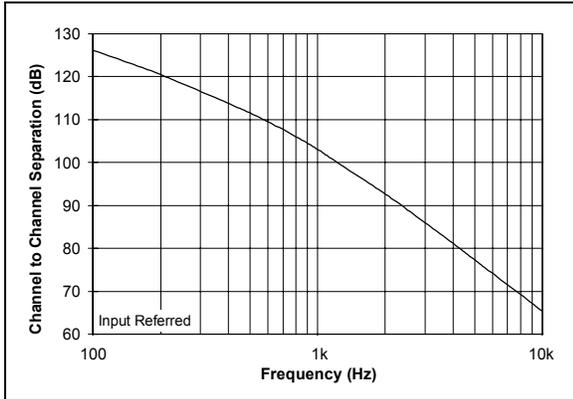
**FIGURE 2-21:** Open Loop Gain vs. Power Supply Voltage.



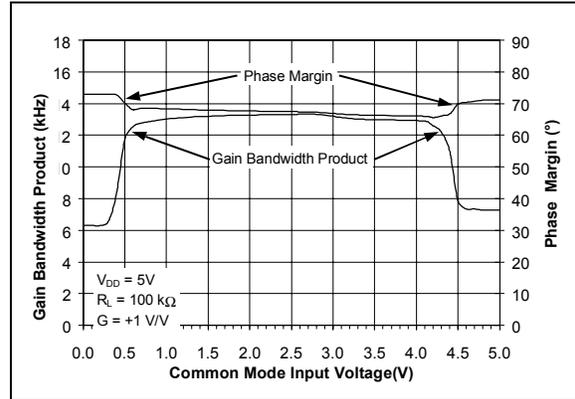
**FIGURE 2-24:** Open Loop Gain vs. Output Voltage Headroom vs. Power Supply Voltage.

# MCP6041/2/3/4

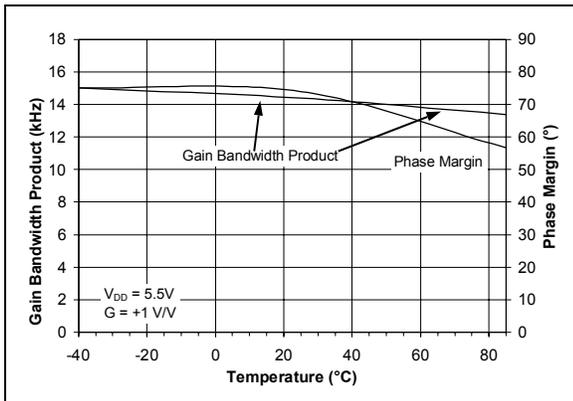
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



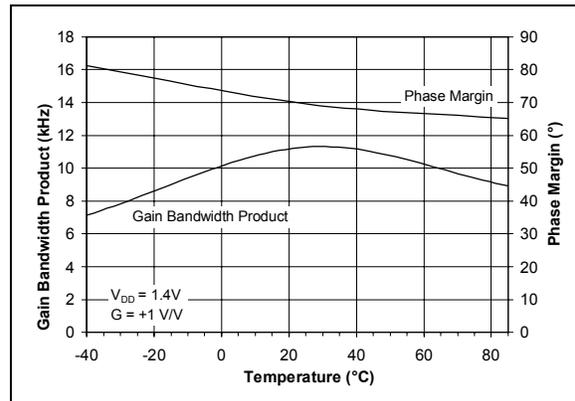
**FIGURE 2-25:** Channel to Channel Separation vs. Frequency (MCP6042 and MCP6044 only).



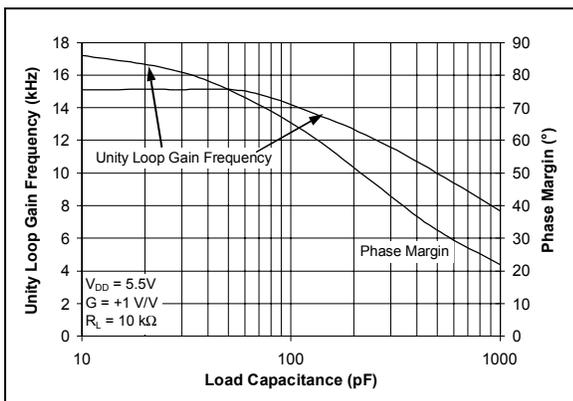
**FIGURE 2-28:** Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage with Unity Gain.



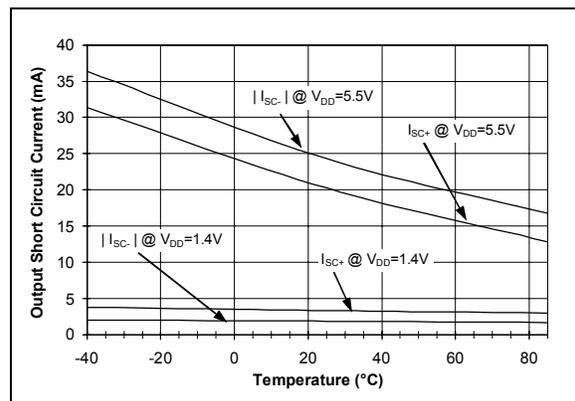
**FIGURE 2-26:** Gain Bandwidth Product, Phase Margin vs. Temperature with  $V_{DD} = 5.5\text{ V}$ , Unity Gain.



**FIGURE 2-29:** Gain Bandwidth Product, Phase Margin vs. Temperature with  $V_{DD} = 1.4\text{ V}$ , Unity Gain.

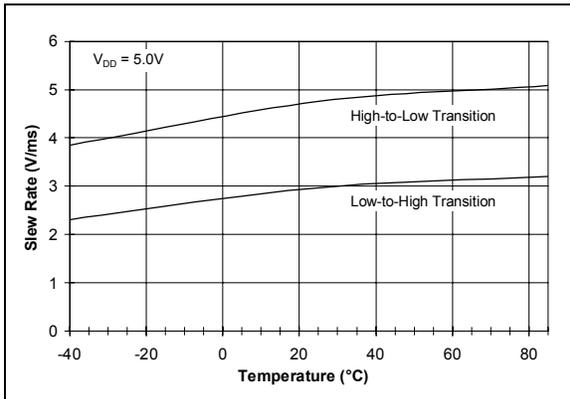


**FIGURE 2-27:** Unity Loop Gain Frequency, Phase Margin vs. Load Capacitance.

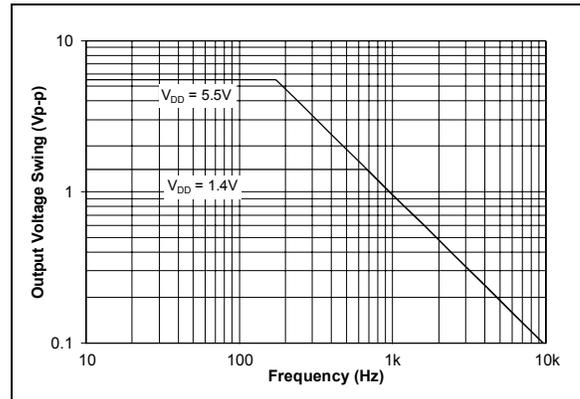


**FIGURE 2-30:** Output Short Circuit Current vs. Temperature vs. Power Supply Voltage.

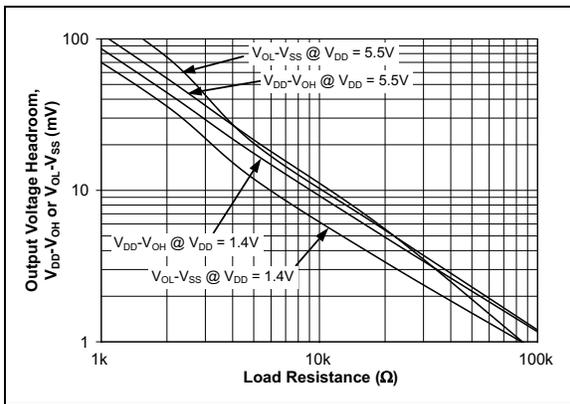
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



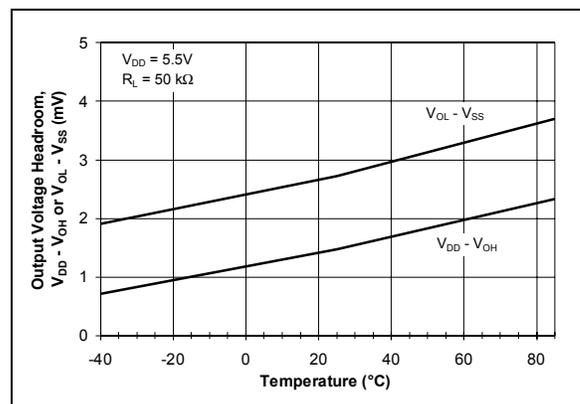
**FIGURE 2-31:** Slew Rate vs. Temperature.



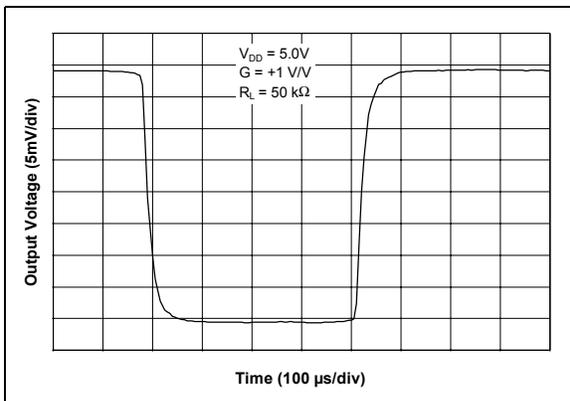
**FIGURE 2-34:** Output Voltage Swing vs. Frequency vs. Power Supply Voltage.



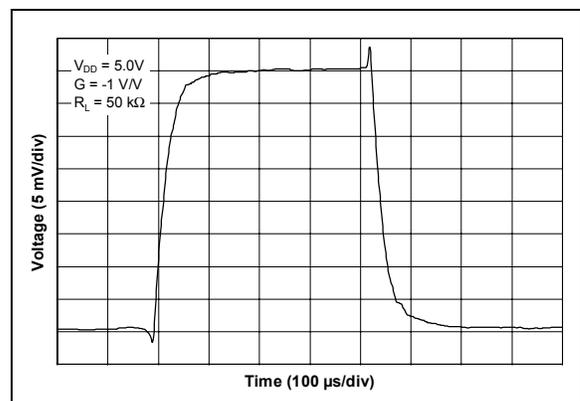
**FIGURE 2-32:** Output Voltage Headroom vs. Load Resistance vs. Power Supply Voltage.



**FIGURE 2-35:** Output Voltage Headroom vs. Temperature.



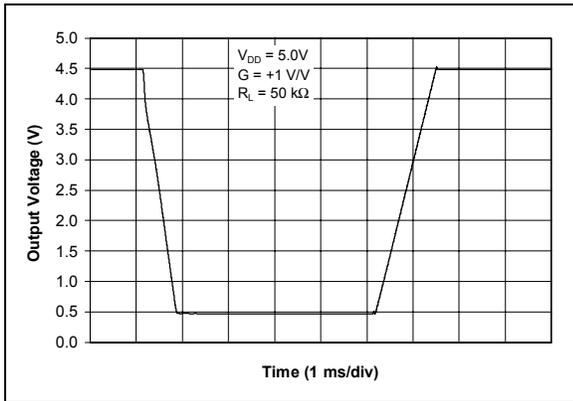
**FIGURE 2-33:** Small Signal Non-Inverting Pulse Response.



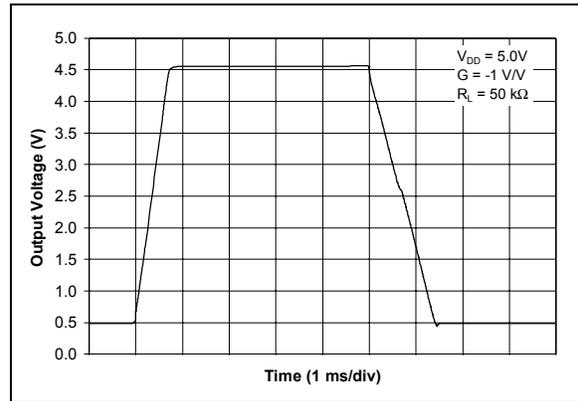
**FIGURE 2-36:** Small Signal Inverting Pulse Response.

# MCP6041/2/3/4

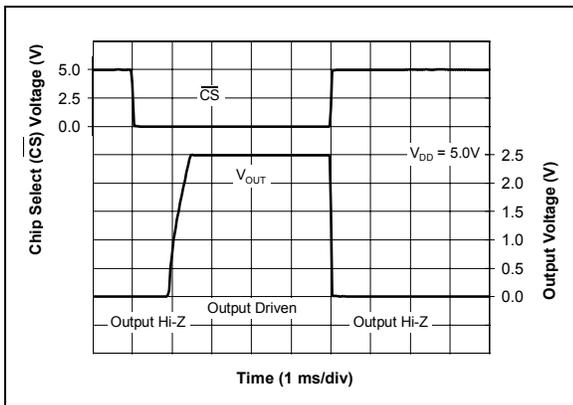
**Note:** Unless otherwise indicated,  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = 1\text{ M}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $V_{OUT} \sim V_{DD}/2$ .



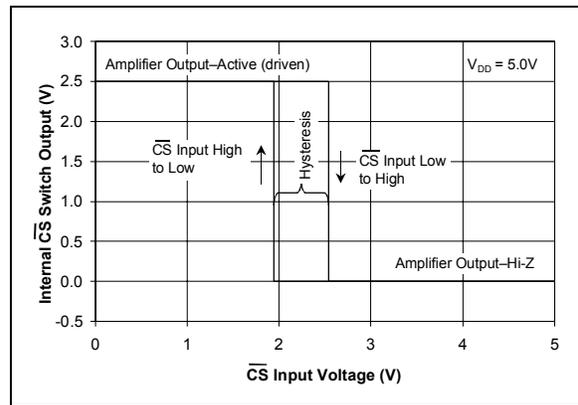
**FIGURE 2-37:** Large Signal Non-Inverting Pulse Response.



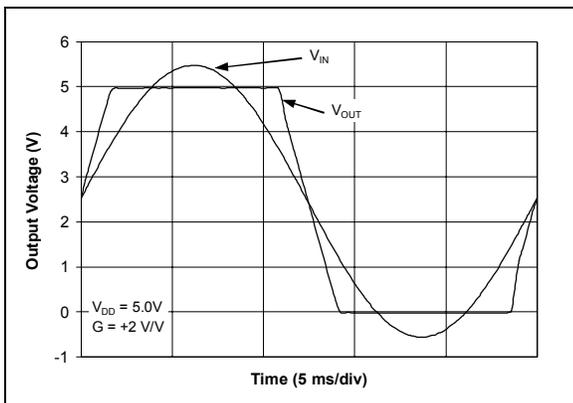
**FIGURE 2-40:** Large Signal Inverting Pulse Response.



**FIGURE 2-38:** Chip Select ( $\overline{\text{CS}}$ ) to Amplifier Output Response Time (MCP6043 only).



**FIGURE 2-41:** Chip Select ( $\overline{\text{CS}}$ ) Hysteresis (MCP6043 only).



**FIGURE 2-39:** The MCP6041/2/3/4 family shows no phase reversal (for information only—the Maximum Absolute Input Voltage is still  $V_{SS}-0.3\text{ V}$  and  $V_{DD}+0.3\text{ V}$ ).

## 3.0 APPLICATIONS INFORMATION

The MCP6041/2/3/4 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are unity gain stable and suitable for a wide range of applications requiring very low power consumption. With these op amps, the power supply pin needs to be by-passed with a 0.1  $\mu\text{F}$  capacitor.

### 3.1 Rail to Rail Input

The input stage of the family of devices uses two differential input stages in parallel; one operates at low  $V_{\text{CM}}$  (common mode input voltage) and the other at high  $V_{\text{CM}}$ . With this topology, the MCP6041/2/3/4 family operates with  $V_{\text{CM}}$  up to 300 mV past either supply rail. The Input Offset Voltage is measured at both  $V_{\text{CM}} = V_{\text{SS}} - 0.3 \text{ V}$  and  $V_{\text{DD}} + 0.3 \text{ V}$  to ensure proper operation.

### 3.2 Output Loads and Battery Life

The MCP6041/2/3/4 op amp family has outstanding quiescent current, which supports battery-powered applications. There is minimal quiescent current glitching when chip select ( $\overline{\text{CS}}$ ) is raised or lowered. This prevents excessive current draw and reduced battery life, when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5 V across a 100 k $\Omega$  load resistor will cause the supply current to increase by 25  $\mu\text{A}$ , depleting the battery 43 times as fast as  $I_{\text{Q}}$  (0.6  $\mu\text{A}$  typ) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1  $\mu\text{F}$  capacitor at the output presents an AC impedance of 15.9 k $\Omega$  ( $1/2\pi fC$ ) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 Vp-p sinewave (1.77 Vrms), under these conditions, is:

#### EQUATION

$$\begin{aligned} P_{\text{SUPPLY}} &= (V_{\text{DD}} - V_{\text{SS}})(I_{\text{Q}} + V_{\text{L}(p-p)}fC_{\text{L}}) \\ &= (5\text{V})(0.6\mu\text{A} + 5.0\text{V}_{p-p} \cdot 100\text{Hz} \cdot 0.1\mu\text{F}) \\ &= 3.0\mu\text{W} + 50\mu\text{W} \end{aligned}$$

This will drain the battery 18 times as fast as  $I_{\text{Q}}$  alone.

### 3.3 Rail to Rail Output

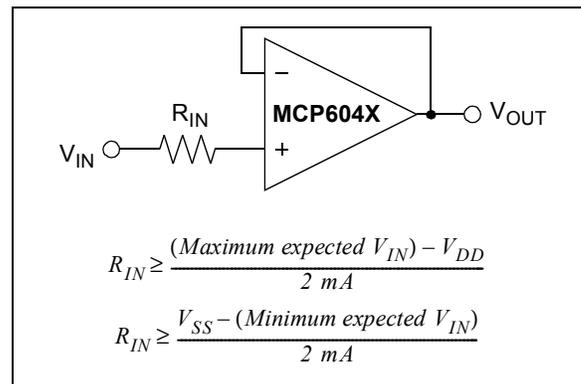
The output voltage range of the MCP6041/2/3/4 family is specified two ways. The first specification, Maximum Output Voltage Swing, defines the maximum swing possible under a particular output load. According to the spec table, the output can reach  $\leq 10 \text{ mV}$  of either supply rail when  $R_{\text{L}} = 50 \text{ k}\Omega$ . See Figure 2-32 for information on Maximum Output Voltage Swing vs. load resistance.

The second specification, Linear Region Output Voltage Swing, details the output voltage range that supports the specified Open Loop Gain ( $A_{\text{OL}} \geq 95 \text{ dB}$  with  $R_{\text{L}} = 50 \text{ k}\Omega$ ).

### 3.4 Input Voltage and Phase Reversal

The MCP6041/2/3/4 op amp family uses CMOS transistors at the input. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-39 shows an input voltage exceeding both supplies with no resulting phase inversion.

The maximum operating  $V_{\text{CM}}$  (common mode input voltage) that can be applied to the inputs is  $V_{\text{SS}} - 0.3 \text{ V}$  and  $V_{\text{DD}} + 0.3 \text{ V}$ . Voltage on the input that exceed this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond  $\pm 2 \text{ mA}$  can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor as shown in Figure 3-1.



**FIGURE 3-1:** An input resistor,  $R_{\text{IN}}$ , should be used to limit excessive input current if the inputs exceed the Absolute Maximum specification.

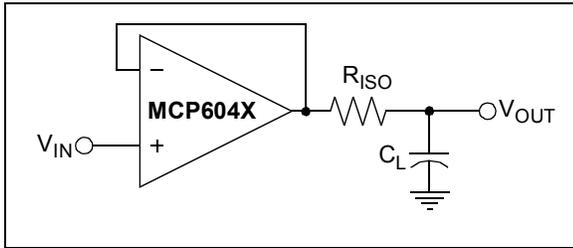
### 3.5 Capacitive Load and Stability

Driving capacitive loads can cause stability problems with voltage feedback op amps. A buffer configuration ( $G = +1$ ) is the most sensitive to capacitive loads. Figure 2-27 shows how increasing the load capacitance will decrease the phase margin. While a phase margin above  $60^\circ$  is ideal,  $45^\circ$  is sufficient. As can be seen, up to  $C_{\text{L}} = 150 \text{ pF}$  can be placed on the MCP6041/2/3/4 op amp outputs without any problems, while 250 pF is usable with a  $45^\circ$  phase margin.

When the op amp is required to drive large capacitive loads ( $C_{\text{L}} > 150 \text{ pF}$ ), a small series resistor ( $R_{\text{ISO}}$  in Figure 3-2) at the output of the amplifier improves the phase margin. This resistor makes the output load resistive at higher frequencies, which improves the phase margin. The bandwidth reduction caused by the capacitive load, however, is not changed. To select  $R_{\text{ISO}}$ , start with 1 k $\Omega$ , then use the MCP6041 SPICE

# MCP6041/2/3/4

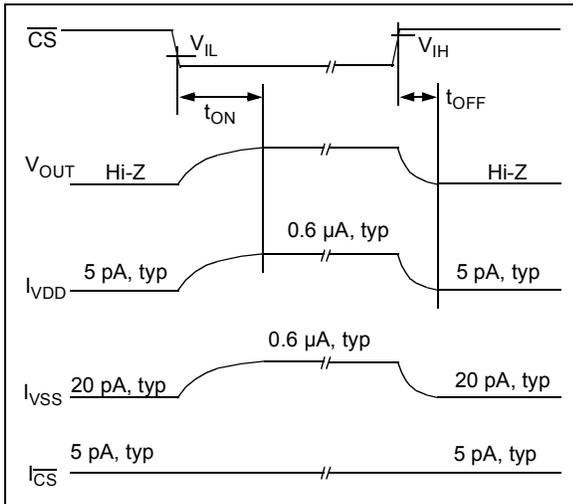
macro model and bench testing to adjust  $R_{ISO}$  until the frequency response peaking is reasonable. Use the smallest reasonable value.



**FIGURE 3-2:** Amplifier circuit for heavy capacitive loads.

## 3.6 The MCP6043 Chip Select ( $\overline{CS}$ ) Option

The MCP6043 is a single amplifier with a chip select ( $\overline{CS}$ ) option. When  $\overline{CS}$  is pulled high, the supply current drops to 20 pA (typ) and goes through the CS pin to  $V_{SS}$ . When this happens, the amplifier is put into a high impedance state. By pulling  $\overline{CS}$  low, the amplifier is enabled. If the  $\overline{CS}$  pin is left floating, the amplifier will not operate properly. Figure 3-3 shows the output voltage and supply current response to a  $\overline{CS}$  pulse.



**FIGURE 3-3:** Timing Diagram for the  $\overline{CS}$  function on the MCP6043 op amp.

## 3.7 Layout Considerations

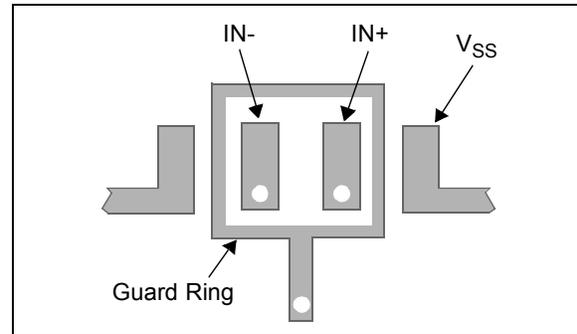
Good PC board layout techniques will help you achieve the performance shown in the specs and Typical Performance Curves. It will also assist in minimizing Electro-Magnetic Compatibility (EMC) issues.

### 3.7.1 SURFACE LEAKAGE

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace to trace need to be considered.

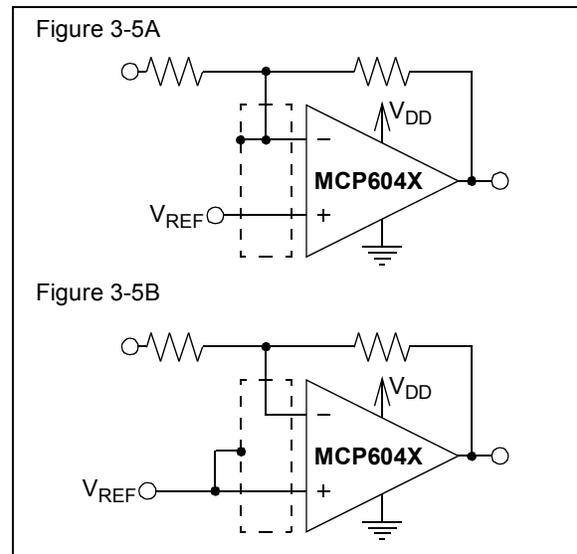
Surface leakage is caused by a difference in voltage between traces, combined with high humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5 V difference would cause 5 pA of current to flow; this is greater than the input current of the MCP6041/2/3/4 family at 25°C (1 pA, typ).

The simplest technique to reduce surface leakage is using a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin or trace. Figure 3-4 shows an example of a typical layout.



**FIGURE 3-4:** Example of Guard Ring layout.

Circuit schematics for different guard ring implementations are shown in Figure 3-5. Figure 3-5A biases the guard ring to the input common mode voltage, which is most effective for non-inverting gains, including unity gain. Figure 3-5B biases the guard ring to a reference voltage ( $V_{REF}$ , which can be ground). This is useful for inverting gains and precision photo sensing circuits.



**FIGURE 3-5:** Two possible guard ring connection strategies to reduce surface leakage effects.

## 3.7.2 COMPONENT PLACEMENT

Separate digital from analog and low speed from high speed. This helps prevent crosstalk.

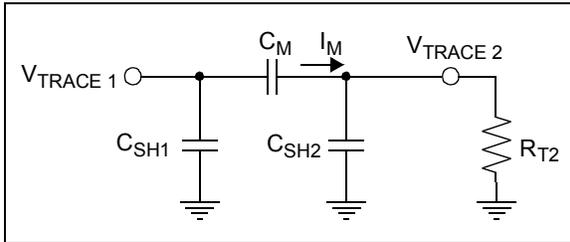
Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.

Use a 0.1  $\mu\text{F}$  supply bypass capacitor within 0.1" (2.5 mm) of the  $V_{DD}$  pin. It must connect directly to the ground plane.

## 3.7.3 SIGNAL COUPLING

The input pins of the MCP6041/2/3/4 family of op amps are high impedance, which allows noise injection. This noise can be capacitively or magnetically coupled. In either case, using a ground plane helps reduce noise injection.

When noise is coupled capacitively, the ground plane provides shunt capacitance to ground for high frequency signals. Figure 3-6 shows the equivalent circuit. The coupled current,  $I_M$ , produces a lower voltage ( $V_{\text{TRACE 2}}$ ) on the victim trace when the trace to ground plane capacitance ( $C_{\text{SH2}}$ ) is large and the terminating resistor ( $R_{\text{T2}}$ ) is small. Increasing the distance between traces, and using wider traces, also helps.



**FIGURE 3-6:** Equivalent circuit for capacitive coupling between traces on a PC board (with ground plane).

When noise is coupled magnetically, ground plane reduces the mutual inductance between traces. This occurs because the ground return current at high frequencies will follow a path directly beneath the signal trace. Increasing the separation between traces makes a significant difference. Changing the direction of one of the traces can also reduce magnetic coupling.

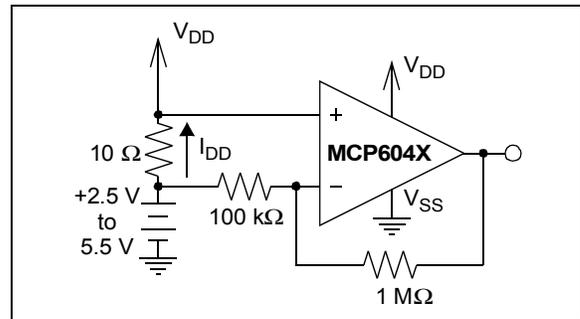
If these techniques are not enough, it may help to place guard traces next to the victim trace. They should be on both sides of the victim trace and be as close as possible. Connect the guard traces to ground plane at both ends, and in the middle, for long traces.

## 3.8 Typical Applications

### 3.8.1 BATTERY CURRENT SENSING

The MCP6041/2/3/4 op amps' Common Mode Input Range, which goes 300 mV beyond both supply rails, supports their use in high side and low side battery current sensing applications. The very low quiescent current (0.6  $\mu\text{A}$ , typ) help prolong battery life while the rail-to-rail output allows you to detect low currents.

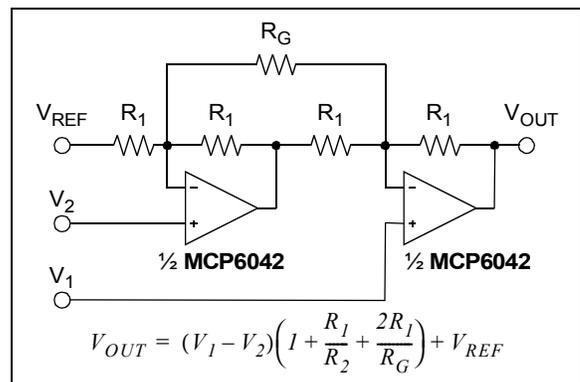
Figure 3-7 shows a high side battery current sensor circuit. The 10  $\Omega$  resistors are sized to minimize power losses. The battery current ( $I_{\text{DD}}$ ) through the 10  $\Omega$  resistor causes its top terminal to be more negative than the bottom terminal. This keeps the common mode input voltage of the op amp  $\leq V_{\text{DD}}$ , which is within its allowed range. The output of the op amp can reach  $V_{\text{DD}} - 0.1$  mV (see Figure 2-32), which is a smaller error than the offset voltage.



**FIGURE 3-7:** High Side Battery Current Sensor.

### 3.8.2 INSTRUMENTATION AMPLIFIER

The MCP6041/2/3/4 op amp is well suited for conditioning sensor signals in battery-powered applications. Figure 3-8 shows a two op amp instrumentation amplifier, using the MCP6042, that works well for applications requiring rejection of common mode noise at higher gains. The reference voltage ( $V_{\text{REF}}$ ) is supplied by a low impedance source. In single supply applications,  $V_{\text{REF}}$  is typically  $V_{\text{DD}}/2$ .



**FIGURE 3-8:** Two Op Amp Instrumentation Amplifier.

$$V_{\text{OUT}} = (V_1 - V_2) \left( 1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G} \right) + V_{\text{REF}}$$

# MCP6041/2/3/4

---

## 4.0 SPICE MACRO MODEL

The Spice macro model for the MCP6041, MCP6042, MCP6043 and MCP6044 simulates the typical amplifier performance of: offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open loop gain over frequency, phase margin, output swing, DC power supply current, power supply current change with supply voltage, input common mode range, output voltage range vs. load and input voltage noise.

The characteristics of the MCP6041, MCP6042, MCP6043 and MCP6044 amplifiers are similar in terms of performance and behavior. This single op amp macro model supports all four devices with the exception of the chip select function of the MCP6043, which is not modeled.

The listing for this macro model is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at [www.microchip.com](http://www.microchip.com)

## Software License Agreement

The software supplied herewith by Microchip Technology Incorporated (the "Company") is intended and supplied to you, the Company's customer, for use solely and exclusively on Microchip products.

The software is owned by the Company and/or its supplier, and is protected under applicable copyright laws. All rights are reserved. Any use in violation of the foregoing restrictions may subject the user to criminal sanctions under applicable laws, as well as to civil liability for the breach of the terms and conditions of this license.

THIS SOFTWARE IS PROVIDED IN AN "AS IS" CONDITION. NO WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE APPLY TO THIS SOFTWARE. THE COMPANY SHALL NOT, IN ANY CIRCUMSTANCES, BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, FOR ANY REASON WHATSOEVER.

```
.SUBCKT MCP6041 1 2 3 4 5
*      | | | | |
*      | | | | Output
*      | | | Negative Supply
*      | | Positive Supply
*      | Inverting Input
*      Non-inverting Input
*
* Macromodel for the MCP6041/2/3/4 op amp
family:
* MCP6041 (single)
* MCP6042 (dual)
* MCP6043 (single w/ CS; chip select is not
modeled)
* MCP6044 (quad)
*
* Revision History:
* REV A: 7-9-01 created KEB
*
* Recommendations:
* Use PSpice (other simulators may require
translation)
* For a quick, effective design, use a com-
bination of: data sheet
* specs, bench testing, and simulations
with this macromodel
* For high impedance circuits, set
GMIN=100F in the.OPTIONS
* statement
*
* Supported:
* Typical performance at room temperature
(25 degrees C)
* DC, AC, Transient, and Noise analyses.
* Most specs, including: offsets, PSRR,
CMRR, input impedance,
* open loop gain, voltage ranges, supply
current,..., etc.
*
* Not Supported:
* Chip Select (MCP6043)
* Variation in specs vs. Power Supply Volt-
age
* Distortion (detailed non-linear behavior)
* Temperature analysis
* Process variation
* Behavior outside normal operating region
*
* Input Stage
V10 3 10 -0.3
R10 10 11 78K
R11 10 12 78K
C11 11 12 4.9P
C12 1 0 6P
E12 1 14 POLY(4) 20 0 21 0 26 0 27 0 1M 1 1
1 1
G12 14 0 POLY(2) 22 0 23 0 1.5P 1U 1U
M12 11 14 15 15 NMI
C13 14 2 3P
M14 12 2 15 15 NMI
G14 2 0 POLY(2) 24 0 25 0 0.5P 1U 1U
C14 2 0 6P
I15 15 4 500N
V16 16 4 0.18
D16 16 15 DL
V13 3 13 0.00
D13 14 13 DL
*
* Noise Sources
I20 21 20 17.2N
D20 20 0 DN1
D21 0 21 DN1
I22 23 22 588U
D22 22 0 DN23
D23 0 23 DN23
I24 25 24 588U
D24 24 0 DN23
D25 0 25 DN23
*
* PSRR and CMRR
G26 0 26 POLY(1) 3 4 110U -20U
R26 26 0 1
G27 0 27 POLY(2) 1 3 2 4 -275U 50U 50U
R27 27 0 1
*
* Open Loop Gain, Slew Rate
G30 0 30 POLY(1) 12 11 0 1MEG
R30 30 0 1
C30 30 0 11.4
G31 0 31 POLY(1) 30 0 0 1
R31 31 0 1
C31 31 0 775N
*
* Output Stage
G40 0 40 POLY(1) 45 5 0 22.7M
D41 40 41 DL
R41 41 0 1K
D42 42 40 DL
R42 42 0 1K
G43 3 0 POLY(1) 41 0 100N 1M
G47 0 4 POLY(1) 42 0 100N -1M
E43 43 0 POLY(1) 3 0 0 1
```

# MCP6041/2/3/4

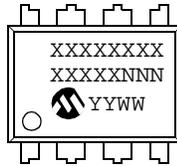
---

```
E47 47 0 POLY(1) 4 0 0 1
V44 43 44 1M
D44 45 44 DLS
D46 46 45 DLS
V46 46 47 1M
G45 47 45 POLY(2) 31 0 3 4 0 8U 4U
R45 45 47 125K
R48 45 5 44
C48 5 0 2P
*
* Models
.MODEL NMI NMOS L=2 W=42
.MODEL DL D N=1 IS=1F
.MODEL DLS D N=1M IS=1F
.MODEL DN1 D IS=1F KF=1.13E-18 AF=1
.MODEL DN23 D IS=1F KF=3E-20 AF=1
*
.ENDS MCP6041
```

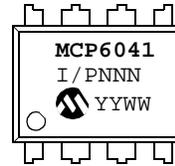
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

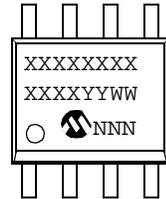
8-Lead PDIP (300 mil)



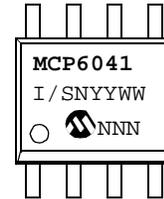
Example:



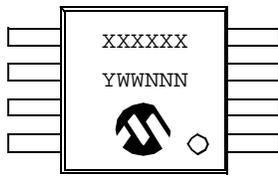
8-Lead SOIC (150 mil)



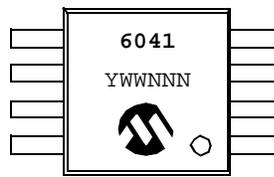
Example:



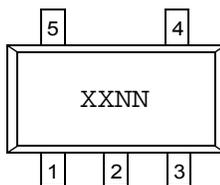
8-Lead MSOP



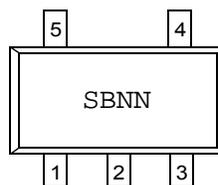
Example:



5-Lead SOT-23 (MCP6041 only)



Example:



<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

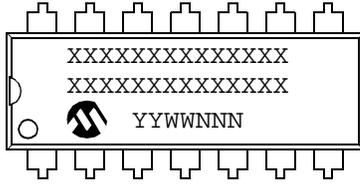
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

\* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

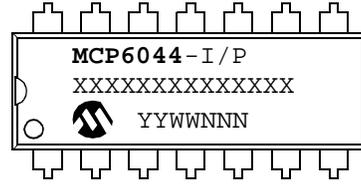
# MCP6041/2/3/4

## 5.1 Package Marking Information (Continued)

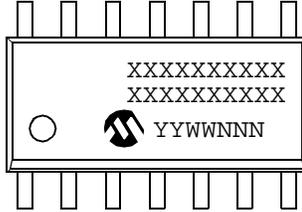
14-Lead PDIP (300 mil) (MCP6044)



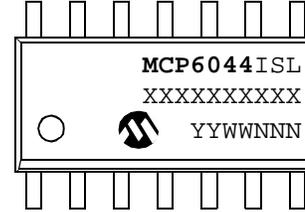
Example:



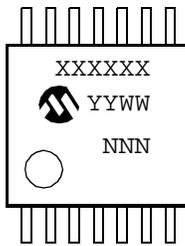
14-Lead SOIC (150 mil) (MCP6044)



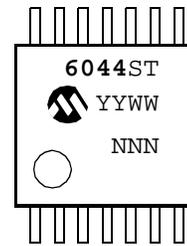
Example:



14-Lead TSSOP (MCP6044)



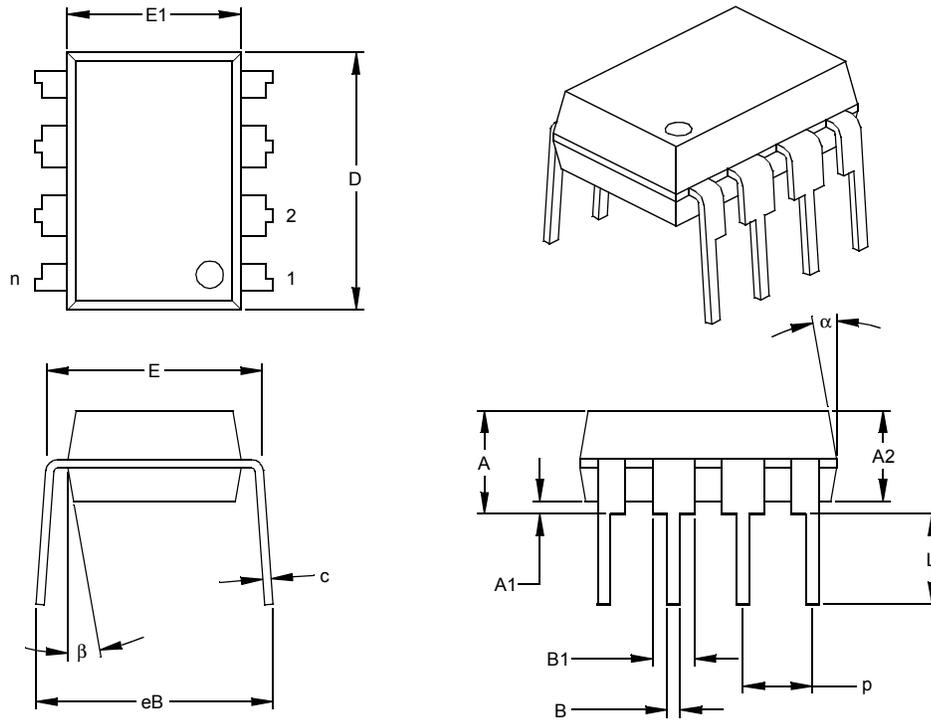
Example:



<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

\* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



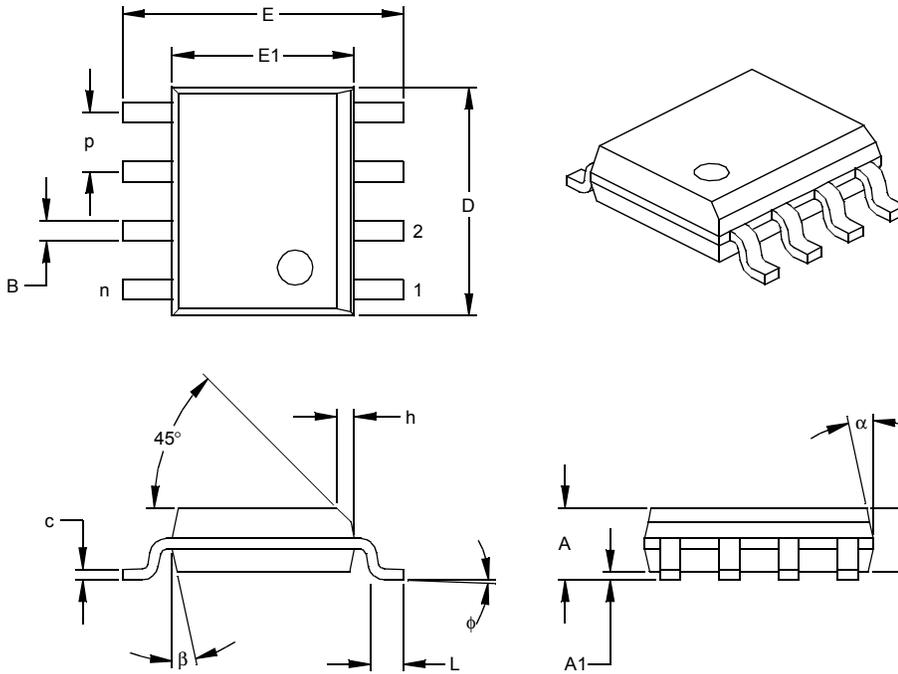
Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-001  
 Drawing No. C04-018

# MCP6041/2/3/4

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

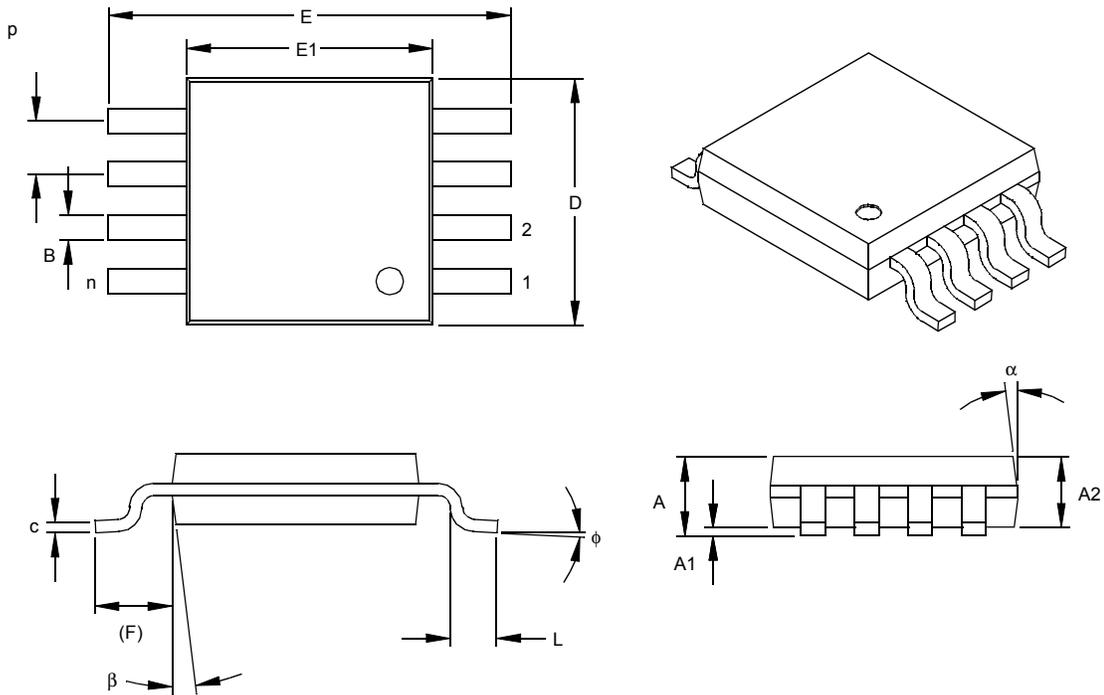
**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

## 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

\*Controlling Parameter  
 § Significant Characteristic

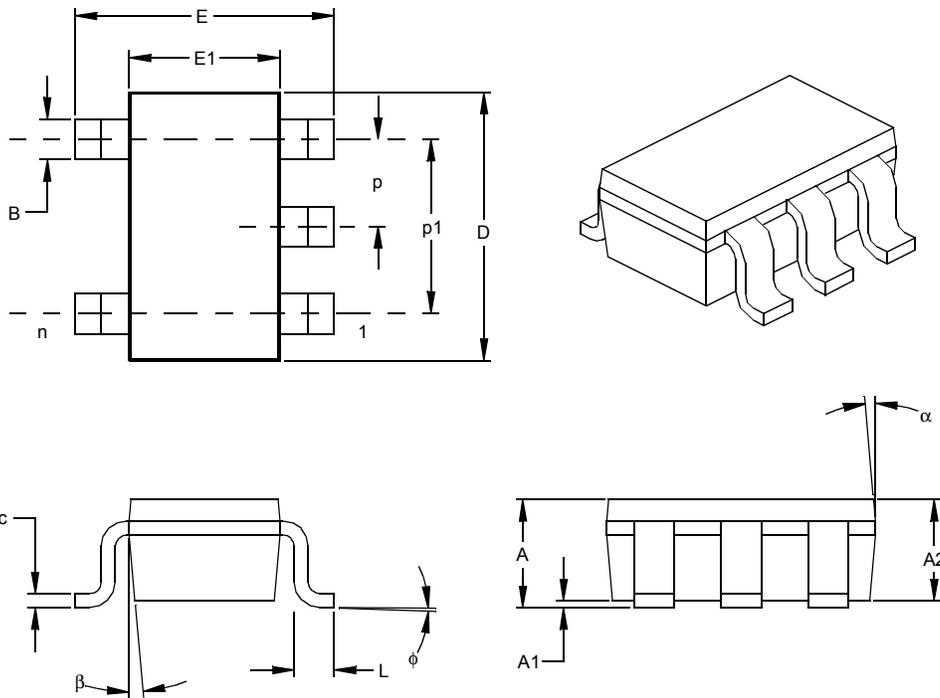
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

# MCP6041/2/3/4

## 5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

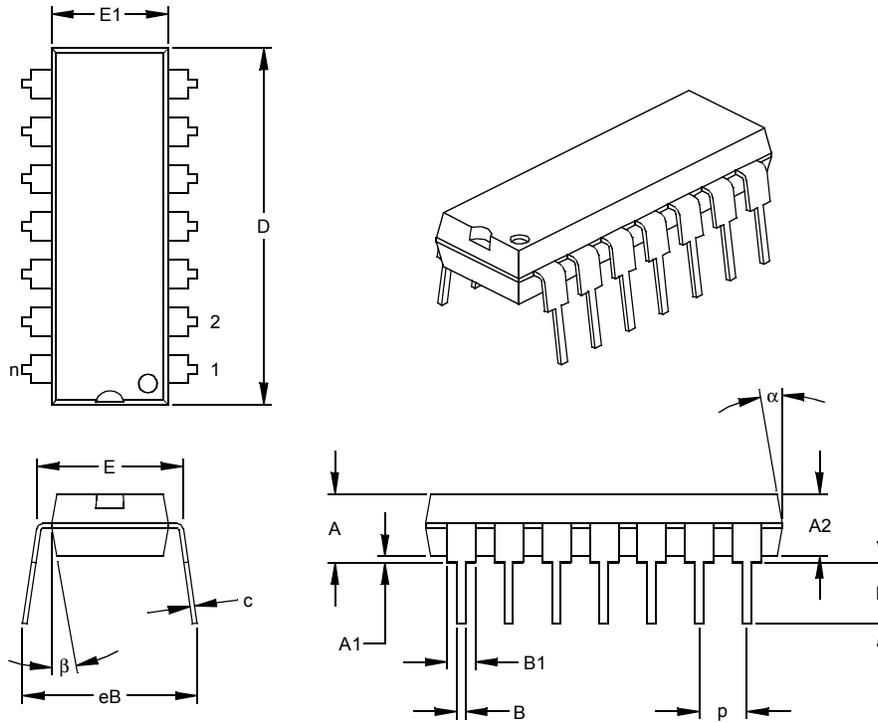
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-178

Drawing No. C04-091

## 14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

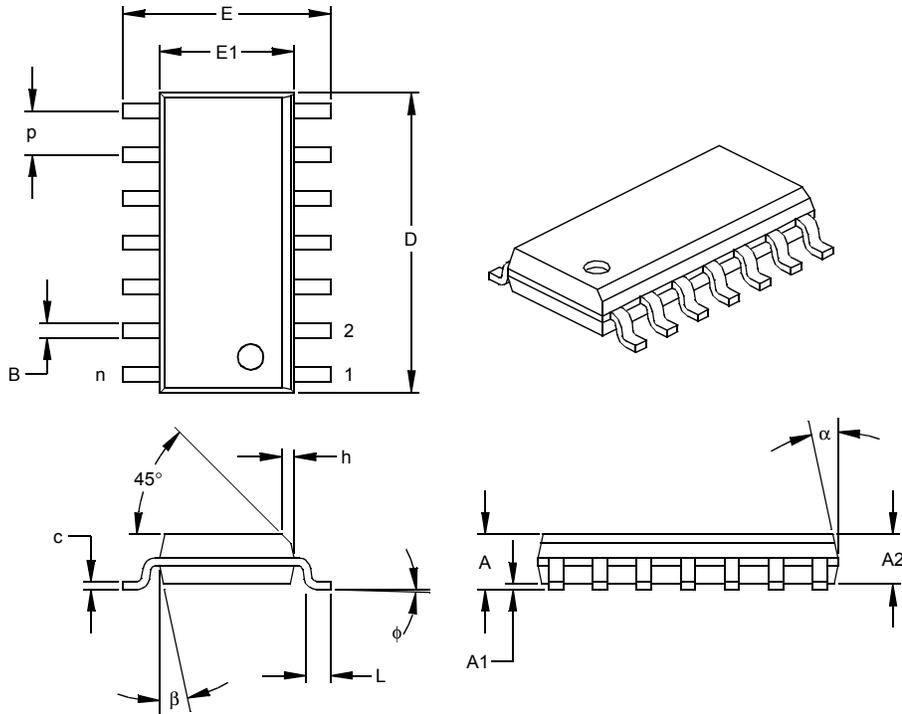
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

# MCP6041/2/3/4

## 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

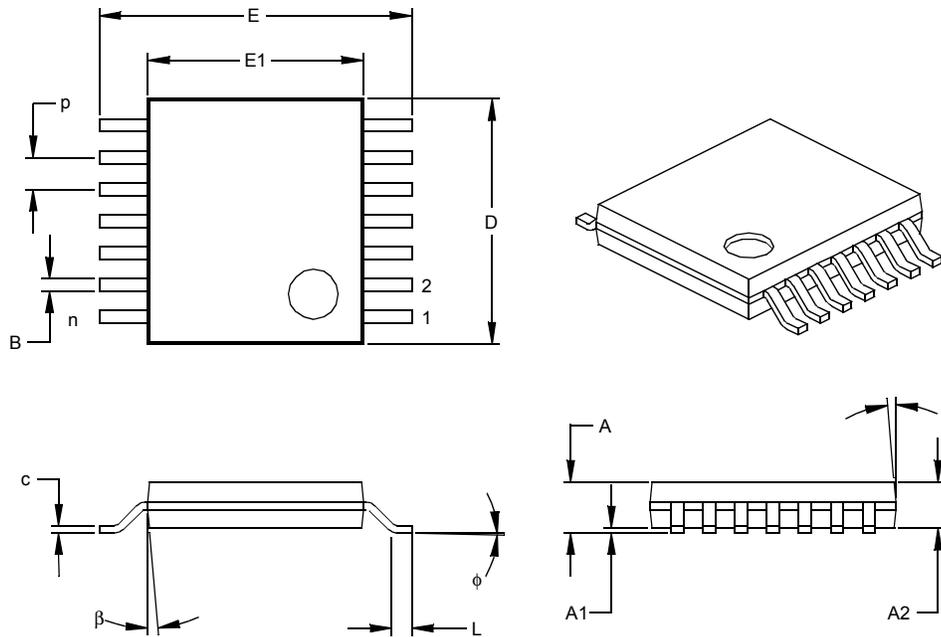
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

# MCP6041/2/3/4

---

NOTES:

## ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

### Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

**[www.microchip.com](http://www.microchip.com)**

The file transfer site is available by using an FTP service to connect to:

**<ftp://ftp.microchip.com>**

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

## Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and  
1-480-792-7302 for the rest of the world.

013001

# MCP6041/2/3/4

---

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager Total Pages Sent  
RE: Reader Response  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: **MCP6041/2/3/4** Literature Number: **DS21669B**

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this data sheet easy to follow? If not, why?

---

---

4. What additions to the data sheet do you think would enhance the structure and subject?

---

---

5. What deletions from the data sheet could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

8. How would you improve our software, systems, and silicon products?

---

---

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device:	MCP6041: CMOS Single Op Amp MCP6041T: CMOS Single Op Amp (Tape and Reel for SOT-23, SOIC, MSOP)	
	MCP6042: CMOS Dual Op Amp MCP6042T: CMOS Dual Op Amp (Tape and Reel for SOIC and TSSOP)	
	MCP6043: CMOS Single Op Amp w/CS Function MCP6043T: CMOS Single Op Amp w/CS Function (Tape and Reel for SOIC and MSOP)	
	MCP6044: CMOS Quad Op Amp MCP6044T: CMOS Quad Op Amp (Tape and Reel for SOIC and TSSOP)	
Temperature Range:	I = -40°C to +85°C	
Package:	MS = Plastic MSOP, 8-lead P = Plastic DIP (300 mil Body), 8-lead, 14-lead SN = Plastic SOIC (150 mil Body), 8-lead OT = Plastic Small Outline Transistor (SOT-23), 5-lead (Tape and Reel - MCP6041 only) SL = Plastic SOIC (150 mil Body), 14-lead ST = Plastic TSSOP (4.4mm Body), 14-lead	

**Examples:**

- a) MCP6041-I/P: Industrial temperature, PDIP package.
- b) MCP6041T-I/OT: Tape and Reel, Industrial temperature, SOT-23 package.
- c) MCP6042-I/SN: Industrial temperature, SOIC package.
- d) MCP6043-I/MS: Industrial temperature, MSOP package.
- e) MCP6044-I/SL: Industrial temperature, SIOC package.
- f) MCP6044-I/ST: Industrial temperature, TSSOP package.

## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

### New Customer Notification System

Register on our web site ([www.microchip.com/cn](http://www.microchip.com/cn)) to receive the most current information on our products.

# MCP6041/2/3/4

---

---

NOTES:

---

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

#### Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

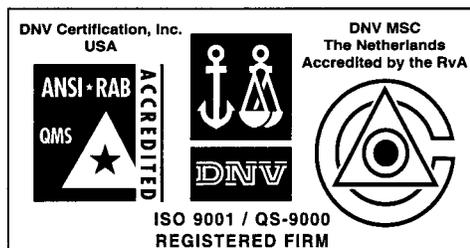
dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, MXLAB, PICC, PICDEM, PICDEM.net, rFPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*



# MICROCHIP

## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200 Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: <http://www.microchip.com>

#### Rocky Mountain

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-692-7966 Fax: 480-792-4338

#### Atlanta

500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770-640-0034 Fax: 770-640-0307

#### Boston

2 Lan Drive, Suite 120  
Westford, MA 01886  
Tel: 978-692-3848 Fax: 978-692-3821

#### Chicago

333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 630-285-0071 Fax: 630-285-0075

#### Dallas

4570 Westgrove Drive, Suite 160  
Addison, TX 75001  
Tel: 972-818-7423 Fax: 972-818-2924

#### Detroit

Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250 Fax: 248-538-2260

#### Kokomo

2767 S. Albright Road  
Kokomo, Indiana 46902  
Tel: 765-864-8360 Fax: 765-864-8387

#### Los Angeles

18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888 Fax: 949-263-1338

#### New York

150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

#### China - Beijing

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Beijing Liaison Office  
Unit 915  
Bei Hai Wan Tai Bldg.  
No. 6 Chaoyangmen Beidajie  
Beijing, 100027, No. China  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Chengdu Liaison Office  
Rm. 2401, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-86766200 Fax: 86-28-86766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Fuzhou Liaison Office  
Unit 28F, World Trade Plaza  
No. 71 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7503506 Fax: 86-591-7503521

#### China - Shanghai

Microchip Technology Consulting (Shanghai)  
Co., Ltd.  
Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### China - Shenzhen

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Shenzhen Liaison Office  
Rm. 1315, 13/F, Shenzhen Kerry Centre,  
Renminnan Lu  
Shenzhen 518001, China  
Tel: 86-755-2350361 Fax: 86-755-2366086

#### China - Hong Kong SAR

Microchip Technology Hongkong Ltd.  
Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaughnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-6334-8870 Fax: 65-6334-8850

### Taiwan

Microchip Technology (Barbados) Inc.,  
Taiwan Branch  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

Microchip Technology Nordic ApS  
Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
Tel: 45 4420 9895 Fax: 45 4420 9910

#### France

Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Microchip Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

#### Austria

Microchip Technology Austria GmbH  
Durisolstrasse 2  
A-4600 Wels  
Austria  
Tel: 43-7242-2244-399  
Fax: 43-7242-2244-393

05/16/02