December 1988

MM54HC4020/MM74HC4020
14-Stage Binary Counter
MM54HC4040/MM74HC4040
12-Stage Binary Counter

General Description

The MM54HC4020/MM74HC4020, MM54HC4040/MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4020 is a 14 stage counter and the 'HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.
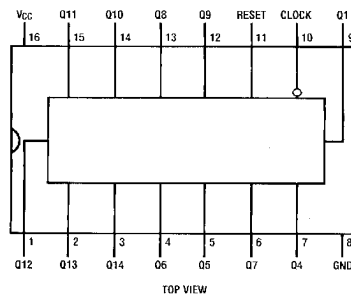
Features

■ Typical propagation delay: 16 ns
■ Wide operating voltage range: 2–6V
■ Low input current: 1 μA maximum
■ Low quiescent current: 80 μA maximum (74HC Series)
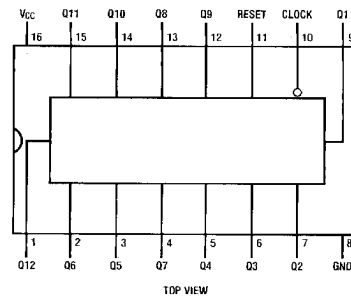■ Output drive capability: 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Packages

'HC4020

TOP VIEW   TL/F/5216-1

'HC4040

TOP VIEW   TL/F/5216-3

Order Number MM54HC4020/4040 or MM74HC4020/4040

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to $+7.0V$
DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5V$
Clamp Diode Current (I_{CD})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	$+85$	°C
MM54HC	-55	$+125$	°C
Input Rise or Fall Times			
(t_r, t_f) $V_{CC}=2.0V$		1000	ns
$V_{CC}=4.5V$		500	ns
$V_{CC}=6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V
			4.5V	3.15	3.15	3.15	V
			6.0V	4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V
			4.5V	1.35	1.35	1.35	V
			6.0V	1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $|I_{OUT}| \leq 20\ \mu A$	2.0V	2.0 1.9	1.9	1.9	V
			4.5V	4.5 4.4	4.4	4.4	V
			6.0V	6.0 5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $|I_{OUT}| \leq 4.0$ mA	4.5V	4.2 3.98	3.84	3.7	V
		$|I_{OUT}| \leq 5.2$ mA	6.0V	5.7 5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $|I_{OUT}| \leq 20\ \mu A$	2.0V	0 0.1	0.1	0.1	V
			4.5V	0 0.1	0.1	0.1	V
			6.0V	0 0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $|I_{OUT}| \leq 4.0$ mA	4.5V	0.2 .26	0.33	0.4	V
		$|I_{OUT}| \leq 5.2$ mA	6.0V	0.2 .26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V	8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

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AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	74HC $T_A = -40$ to 85°C Guaranteed Limits	54HC $T_A = -55$ to 125°C Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	40	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
T_{PHL}, t_{PLH}	Maximum Propagation Delay Between Stages from Q_n to Q_{n+1}		2.0V	80	125	156	188	ns
			4.5V	18	25	31	38	ns
			6.0V	15	21	26	31	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q ('4020 and '4040)		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	126	149	ns
			4.5V		20	25	50	ns
			6.0V		16	21	25	ns
t_W	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: $t_P = 17 + 12(N-1)$ ns; where N is the number of the output, Q_N, at $V_{CC} = 5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.
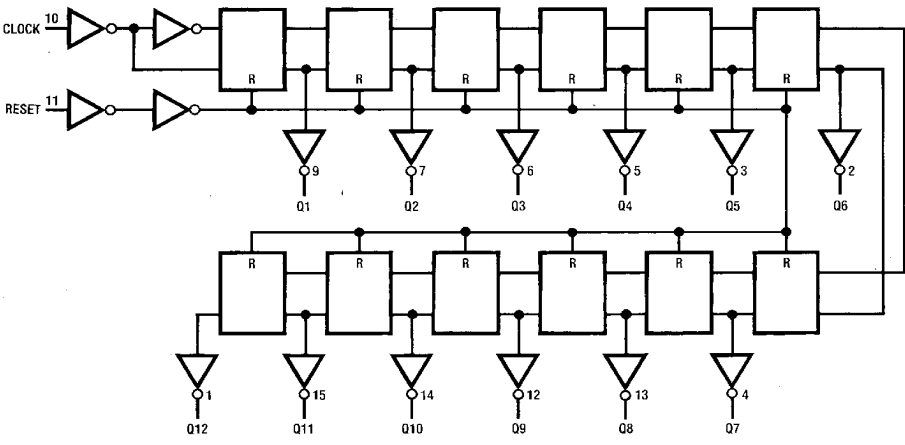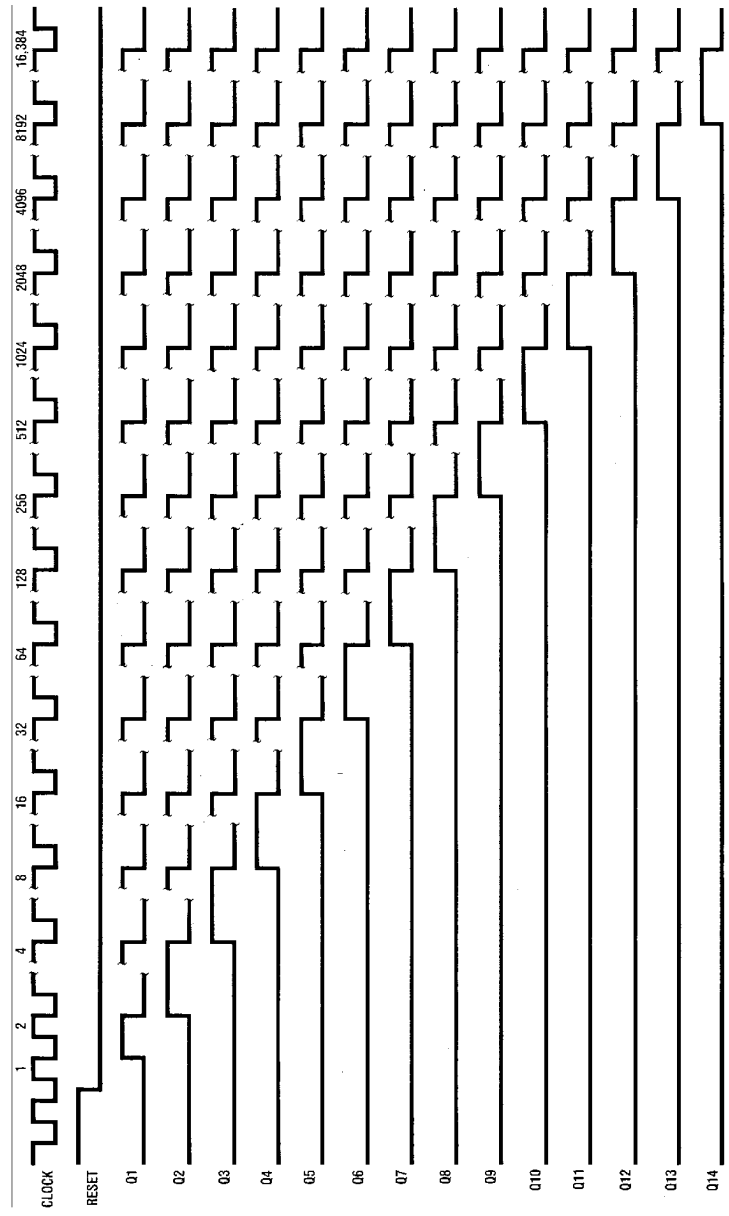
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Logic Diagrams
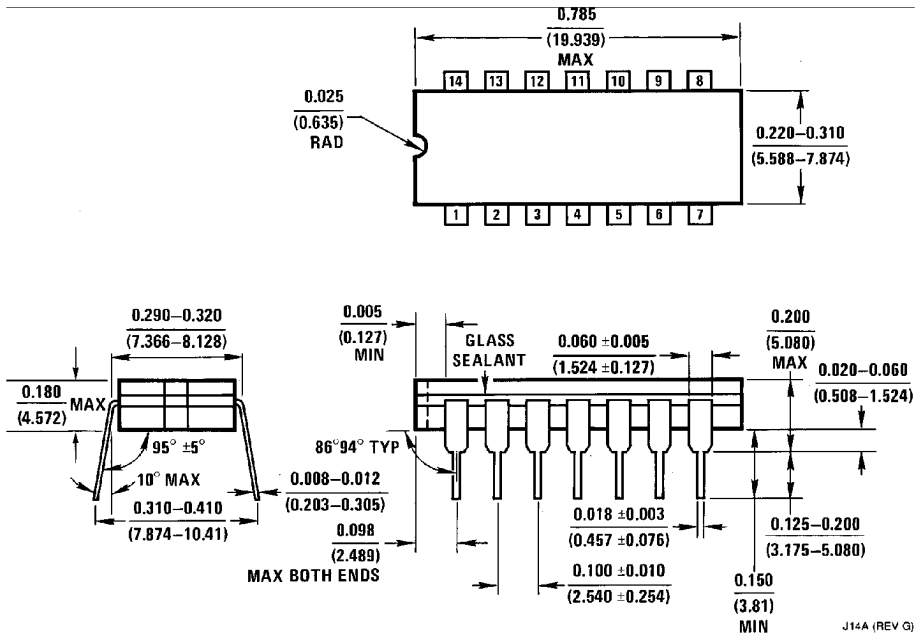
MM54HC4020/MM74HC4020
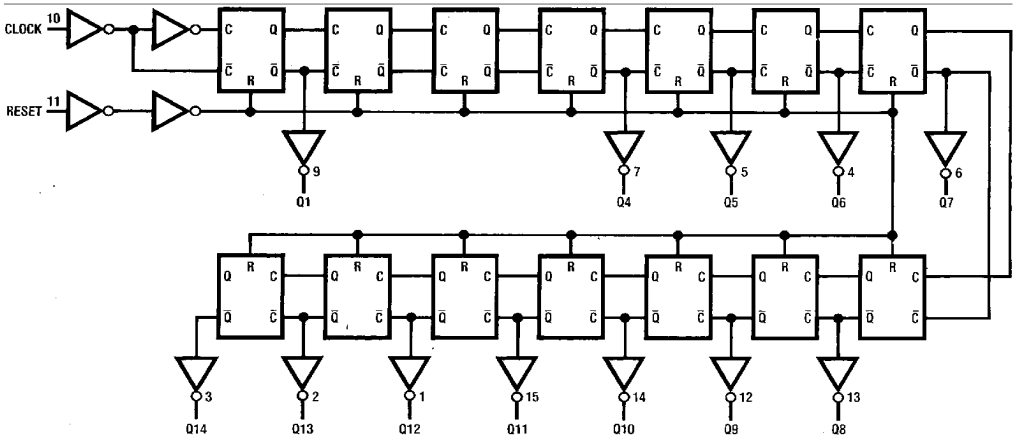
TL/F/5216–5

MM54HC4040/MM74HC4040

TL/F/5216–7

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Timing Diagram

TL/F/5216–11

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Physical Dimensions inches (millimeters)

0.785
(19.939)
MAX

14 13 12 11 10 9 8

0.025
(0.635)
RAD

0.220—0.310
(5.588—7.874)

1 2 3 4 5 6 7

0.290—0.320
(7.366—8.128)

0.005
(0.127)
MIN

GLASS
SEALANT

0.060 ±0.005
(1.524 ±0.127)

0.200
(5.080)
MAX

0.020—0.060
(0.508—1.524)

0.180
(4.572) MAX

95° ±5°

10° MAX

86°—94° TYP

0.008—0.012
(0.203—0.305)

0.310—0.410
(7.874—10.41)

0.098
(2.489)
MAX BOTH ENDS

0.018 ±0.003
(0.457 ±0.076)

0.100 ±0.010
(2.540 ±0.254)

0.125—0.200
(3.175—5.080)

0.150
(3.81)
MIN

J14A (REV G)

**Order Number MM54HC4020J, MM54HC4024J, MM54HC4040J,
MM74HC4020J, MM74HC4024J, or MM74HC4040J
NS Package J14A**

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Physical Dimensions inches (millimeters) (Continued)
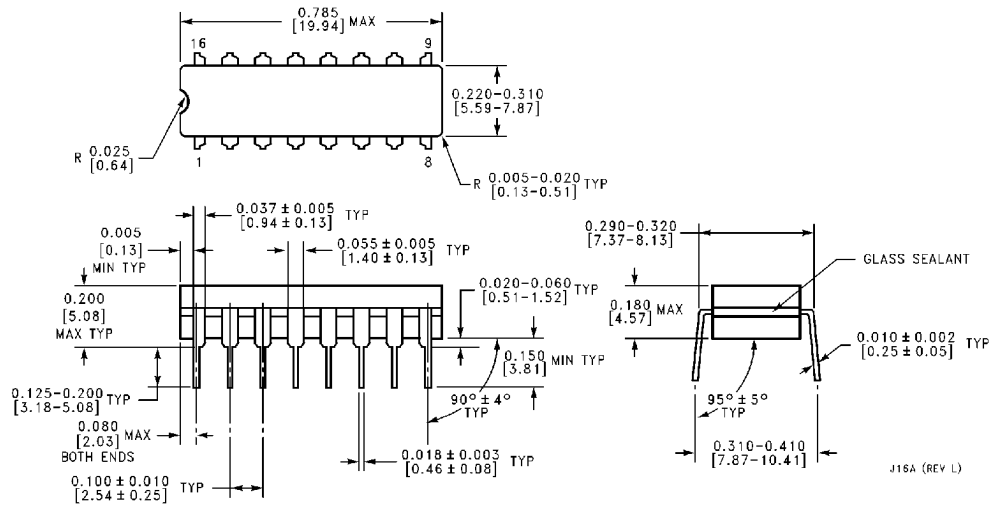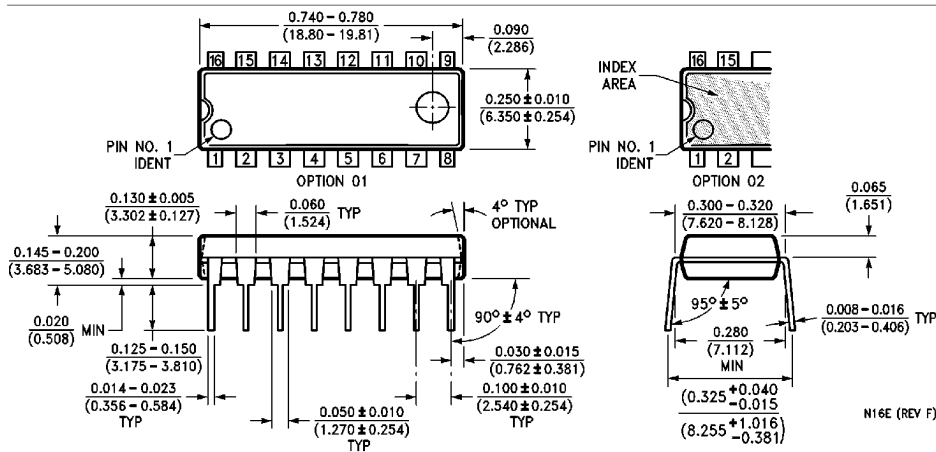

**Order Number MM54HC4020J, MM54HC4024J, MM54HC4040J,
MM74HC4020J, MM74HC4024J, or MM74HC4040J
NS Package J16A**
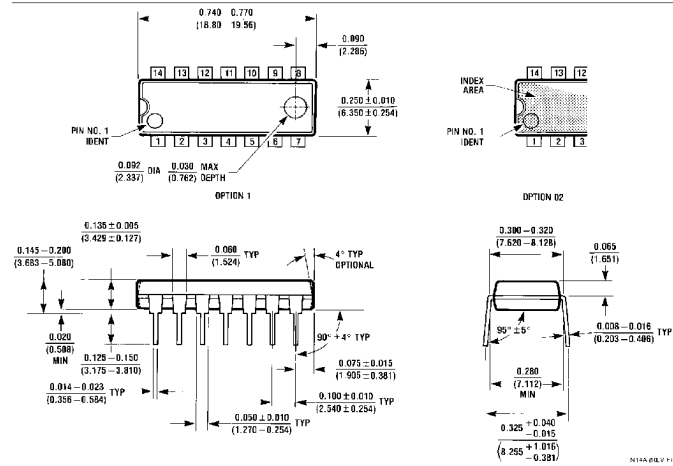
**Order Number MM74HC4020N, MM74HC4024N or MM74HC4040N
NS Package N14A**

Physical Dimensions inches (millimeters) (Continued)

INDEX AREA

PIN NO. 1 IDENT

OPTION 01

OPTION 02

0.740 – 0.780
(18.80 – 19.81)

0.090
(2.286)

0.250 ± 0.010
(6.350 ± 0.254)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP OPTIONAL

0.145 – 0.200
(3.683 – 5.080)

0.020
(0.508) MIN

0.125 – 0.150
(3.175 – 3.810)

90° ± 4° TYP

0.030 ± 0.015
(0.762 ± 0.381)

0.014 – 0.023
(0.356 – 0.584) TYP

0.050 ± 0.010
(1.270 ± 0.254) TYP

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.065
(1.651)

0.300 – 0.320
(7.620 – 8.128)

95° ± 5°

0.280
(7.112) MIN

0.008 – 0.016
(0.203 – 0.406) TYP

$(0.325 ^{+0.040}_{-0.015})$

$(8.255 ^{+1.016}_{-0.381})$

N16E (REV F)

Order Number MM74HC4020N, MM74HC4024N or MM74HC4040N
NS Package N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.