

### STW12NK90Z

# N-channel 900V - 0.72Ω - 11A - TO-247 Zener-protected SuperMESH™ Power MOSFET

### **General features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	p <sub>W</sub>
STW12NK90Z	900V	<0.88Ω	11A	230W

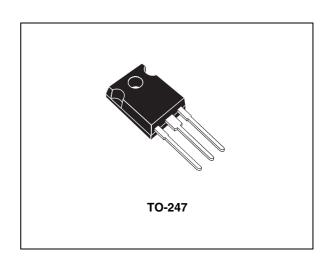
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility

### **Description**

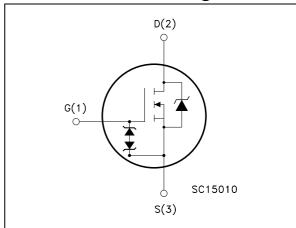
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

### **Applications**

■ Switching application



### Internal schematic diagram



#### **Order codes**

Part number	Marking	Package	Packaging
STW12NK90Z	W12NK90Z	TO-247	Tube

Contents STW12NK90Z

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STW12NK90Z Electrical ratings

# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	900	V
V <sub>GS</sub>	Gate- source voltage	± 30	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	11	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100°C	7	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	44	Α
P <sub>tot</sub>	Total dissipation at T <sub>C</sub> = 25°C	230	W
	Derating Factor	1.85	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
E <sub>AS</sub> (2)	Single pulse avalanche energy	4.5	mJ
T <sub>stg</sub>	Storage temperature	-55 to 150	°C
Tj	Max. operating junction temperature	-55 to 150	O

<sup>1.</sup> Pulse width limited by safe operating area.

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.54	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
$T_J$	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	11	А
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 50$ V)	500	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$BV_GSO$	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

<sup>2.</sup>  $I_{SD} \leq 1A$ , di/dt  $\leq 200A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

Electrical ratings STW12NK90Z

### 1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

# 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1mA, V <sub>GS</sub> =0	900			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	$V_{DS}$ = max rating $V_{DS}$ = max rating, $T_{C}$ = 125°C			1 50	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±10	μА
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\mu A$	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	$V_{GS} = 10V, I_D = 5.5A$		0.72	0.88	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	$V_{DS} = 15V_{,} I_{D} = 5.5A$		11		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		3500 280 58		pF pF pF
C <sub>oss eq</sub> <sup>(2)</sup>	Equivalent output capacitance	$V_{GS} = 0V, V_{DS} = 0V$ to 800V		117		pF
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD}$ = 450V, $I_D$ = 5A $R_G$ = 4.7 $\Omega$ $V_{GS}$ = 10V (see <i>Figure 13</i> )		31 20 88 55		ns ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ = 720V, $I_{D}$ = 10A, $V_{GS}$ = 10V, $R_{G}$ = 4.7 $\Omega$ (see <i>Figure 14</i> )		113 19 60	152	nC nC nC

<sup>1.</sup> Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5 %.

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<sup>2.</sup> Coss eq. is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

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Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current Source-drain current (pulsed)				11 44	A A
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 11A, V <sub>GS</sub> = 0			1.6	V
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 10A$ , di/dt = 100A/ $\mu$ s,		728		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50V, T_j = 25^{\circ}C$		7.8		μC
I <sub>RRM</sub>	Reverse recovery current	(see Figure 15)		21.6		Α
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 10A$ , di/dt = 100A/ $\mu$ s,		964		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50V, T_j = 150^{\circ}C$		11		μC
I <sub>RRM</sub>	Reverse recovery current	(see Figure 15)		23		Α

<sup>1.</sup> Pulse width limited by safe operating area.

<sup>2.</sup> Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5 %

# 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

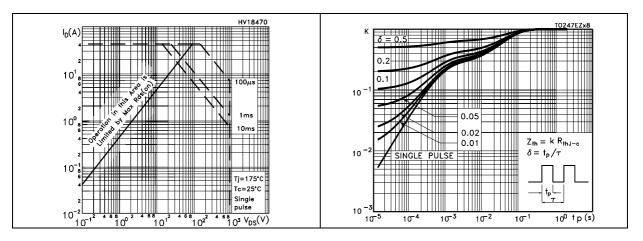


Figure 3. Output characterisics

Figure 4. Transfer characteristics

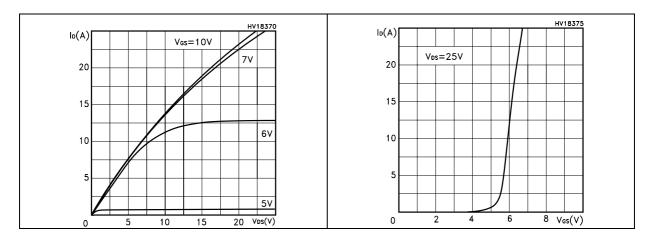
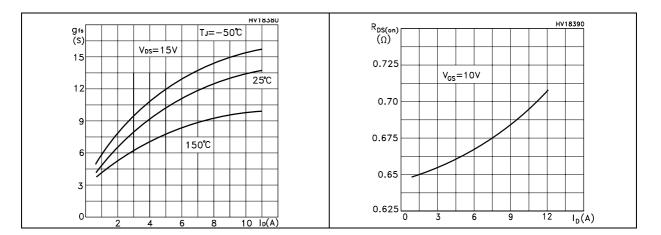


Figure 5. Transconductance

Figure 6. Static drain-source on resistance



Electrical characteristics STW12NK90Z

Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

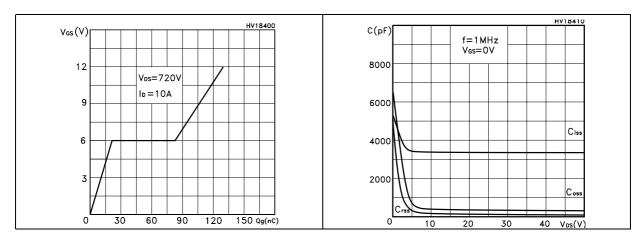


Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on resistance vs temperature

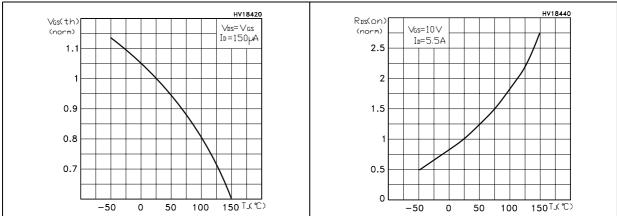
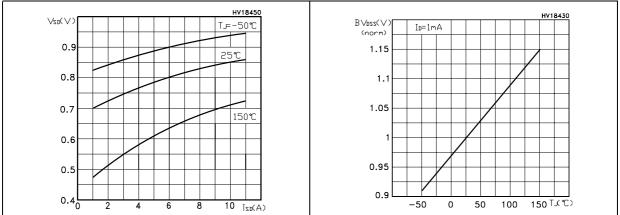


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized breakdown voltage vs temperature



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STW12NK90Z Test circuit

# 3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

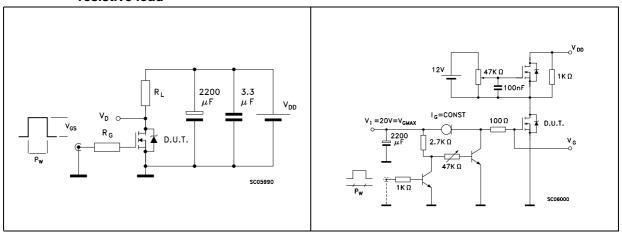
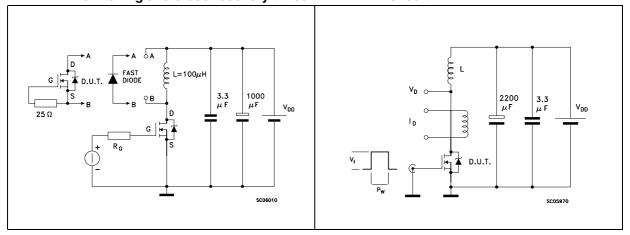


Figure 15. Test circuit for inductive load switching and diode recovery times

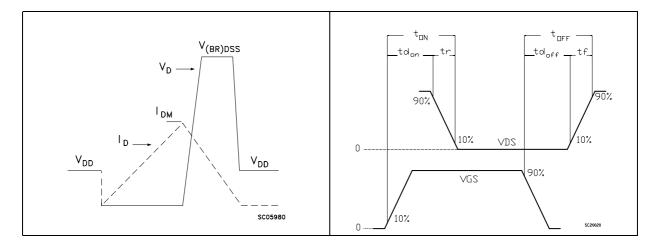
Figure 16. Unclamped Inductive load test circuit



Test circuit STW12NK90Z

Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



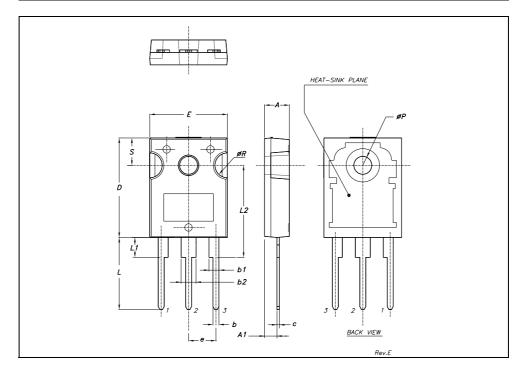
# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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#### **TO-247 MECHANICAL DATA**

DIM.		mm.			inch	
DIIVI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
С	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
е		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øΡ	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



STW12NK90Z Revision history

# 5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete version
17-Oct-2006	5	New template, no content change

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