Data Sheet, April 2001

TDA 16850-2

Free running and synchronized SMPS Controller

Power Management & Supply

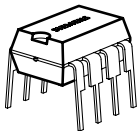
Never stop thinking.

TDA 16850-2

Synchronized SMPS Controller

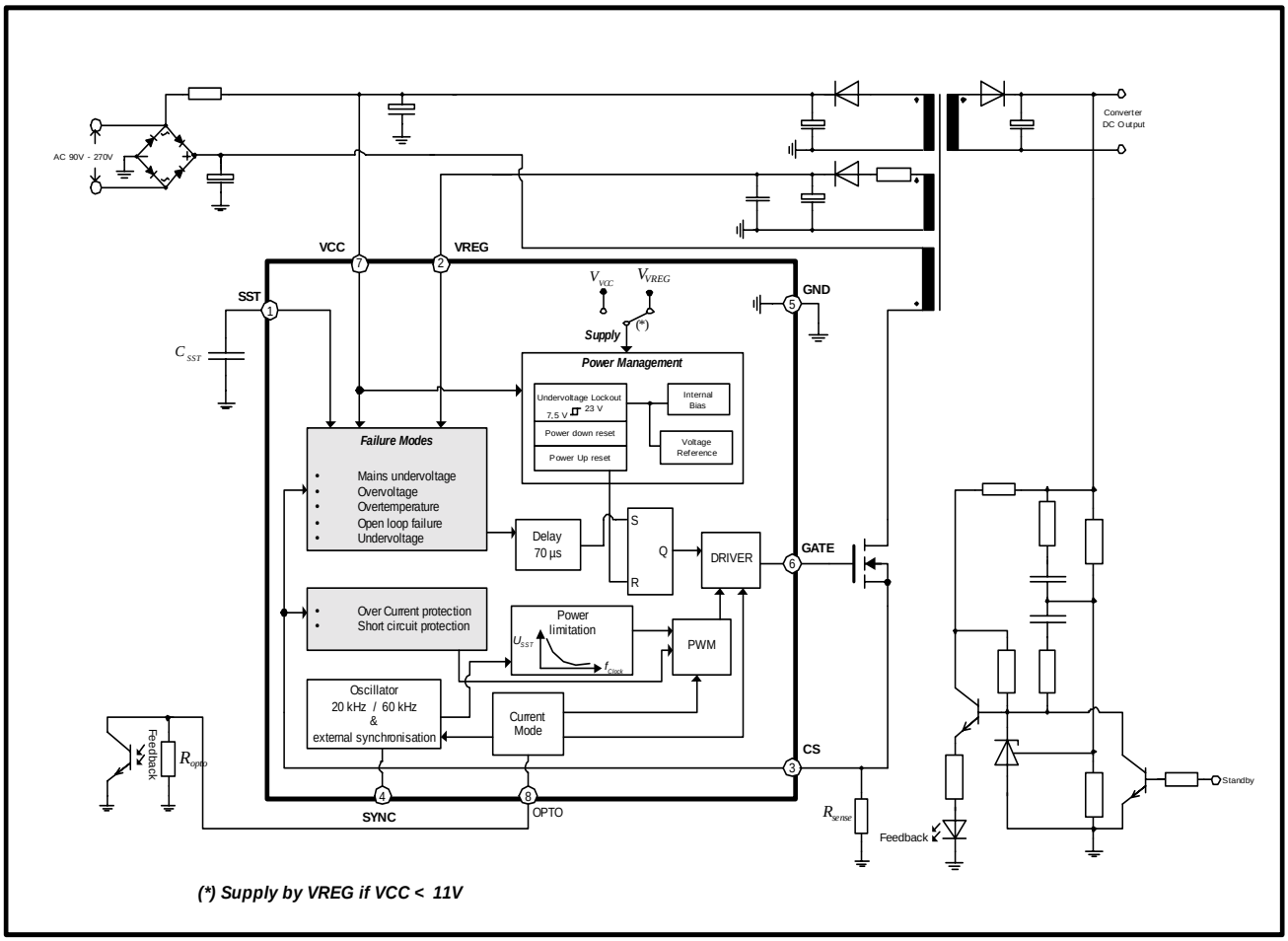
Product Highlights

- **Synchronisation range 30 kHz to 130 kHz**
- **Maximum output power independant of frequency**
- **Standby mode with reduced output voltage by factor 5**
- **Mode changing and voltage feedback through only one optocoupler**
- **Off mode with power consumption less than 250 mW**
- **Standby mode with power consumption less than 1W**
- **Without synchronisation operation with internal oscillator 20kHz/60kHz**
- **Different failure modes recognition with latch function**
- **Minimum external circuitry**



P-DIP-8

Typical application



(*) Supply by VREG if VCC < 11V

Type	Ordering Code	Package
TDA16850-2	Q67040-S4404-A	P-DIP-8

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TDA 16850-2

Synchronized SMPS Controller

1 Overview

1.1 Features

- Controller for Flyback Topology
- Current mode PWM with shunt resistor and spike blanking
- Leading edge triggered pulse width modulation
- Fast, soft switching totem pole gate drive (1 A)
- Soft start management for safe start up

1.2 Special Features

- Typical 100 µA start-up supply current
- Low quiescent current (5 mA)
- Maximum output power independent of frequency
- 20 kHz internal oscillator for start-up and standby mode
- 60 kHz internal oscillator for non synchronized normal mode
- Synchronization range 30 kHz to 130 kHz
- Feedback via optocoupler in normal operation
- Feedback via transformer winding in standby mode
- Standby mode with reduced output voltages by factor of 5
- Off mode with power consumption less then 1 W
- Mode switching and voltage feedback through only one optocoupler
- Different failure modes recognition with latch function

1.3 Protection Features

- Fast and slow peak current limitation
- Mains undervoltage protection
- IC Supply Overvoltage
- IC Supply Undervoltage
- Loop Failure
- Over temperature switch off
- Over current protection
- Short circuit protection

1.4 General Remarks

The TDA 16850-2 comprises the complete control for flyback switched mode power supplies especially in CRT monitors. It also performs all necessary protection functions in flyback converters. The TDA 16850-2 applies to converters with input line voltages ranging from 90 V_{AC} to 270 V_{AC}.

The maximum duty cycle depends on frequency, line voltage and soft start management. The maximum output power therefore will be limited effectively in case of a secondary overload.

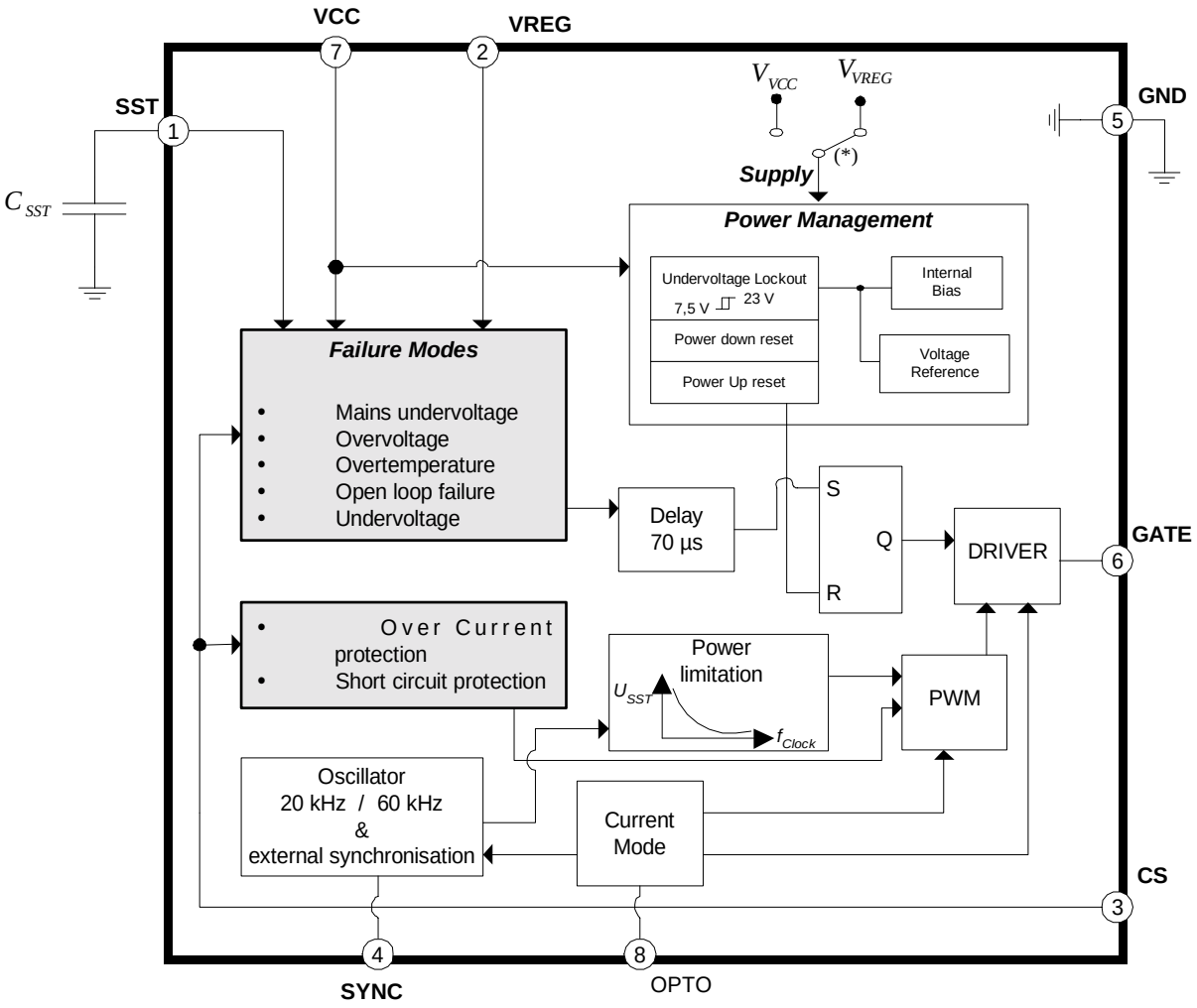
All clock signals as well as the PWM voltage ramp are either synchronized by the internal oscillator or by the synchronisation signal at pin SYNC. The internal oscillator is activated if there is no signal at SYNC. An horizontal deflection signal at pin SYNC synchronizes the internal oscillator automatically.

Mode switching is done via the input current at pin OPTO. In the standby mode the TDA 16850-2 gets its supply from pin VREG. The voltage at VREG is then also the feedback voltage. The TDA 16850-2 will switch off the power supply and enter the off mode when the optocoupler current is completely turned off.

It can restart from a short optocoupler current pulse, which can be derived from a vertical synchronization pulse. The TDA 16850-2 operates in the normal mode if V_{VCC} and I_{OPTO} are in their nominal range.

Type	Ordering Code	Package
TDA16850-2	Q67040-S4404-A	P-DIP-8

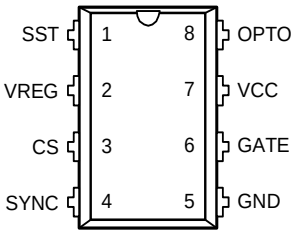
1.5 Block Diagram

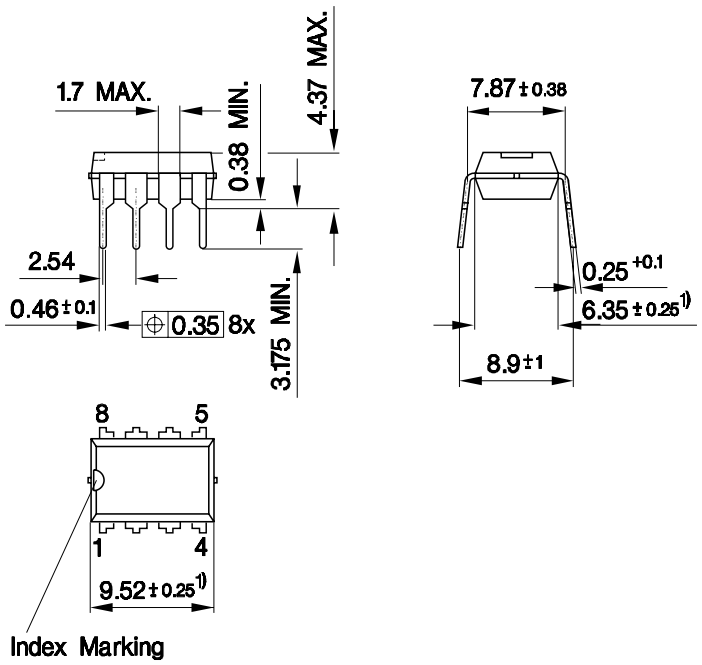


(*) Supply by VREG if VCC < 11V

1.6 Pin Connection and Description

P-DIP-8-4
(Plastic Dual In-line Package)





1) Does not include plastic or metal protrusion of 0.25 max. per side

Pin	Name	Function
1	SST	Soft-start pin for external capacitor C_{SST}
2	VREG	Supply and feedback during standby mode
3	CS	Current sense
4	SYNC	Synchronization input
5	GND	Ground
6	GATE	High current totem pole output
7	VCC	Start up and supply during normal mode
8	OPTO	Feedback and mode switching via input current

2 Functional Description

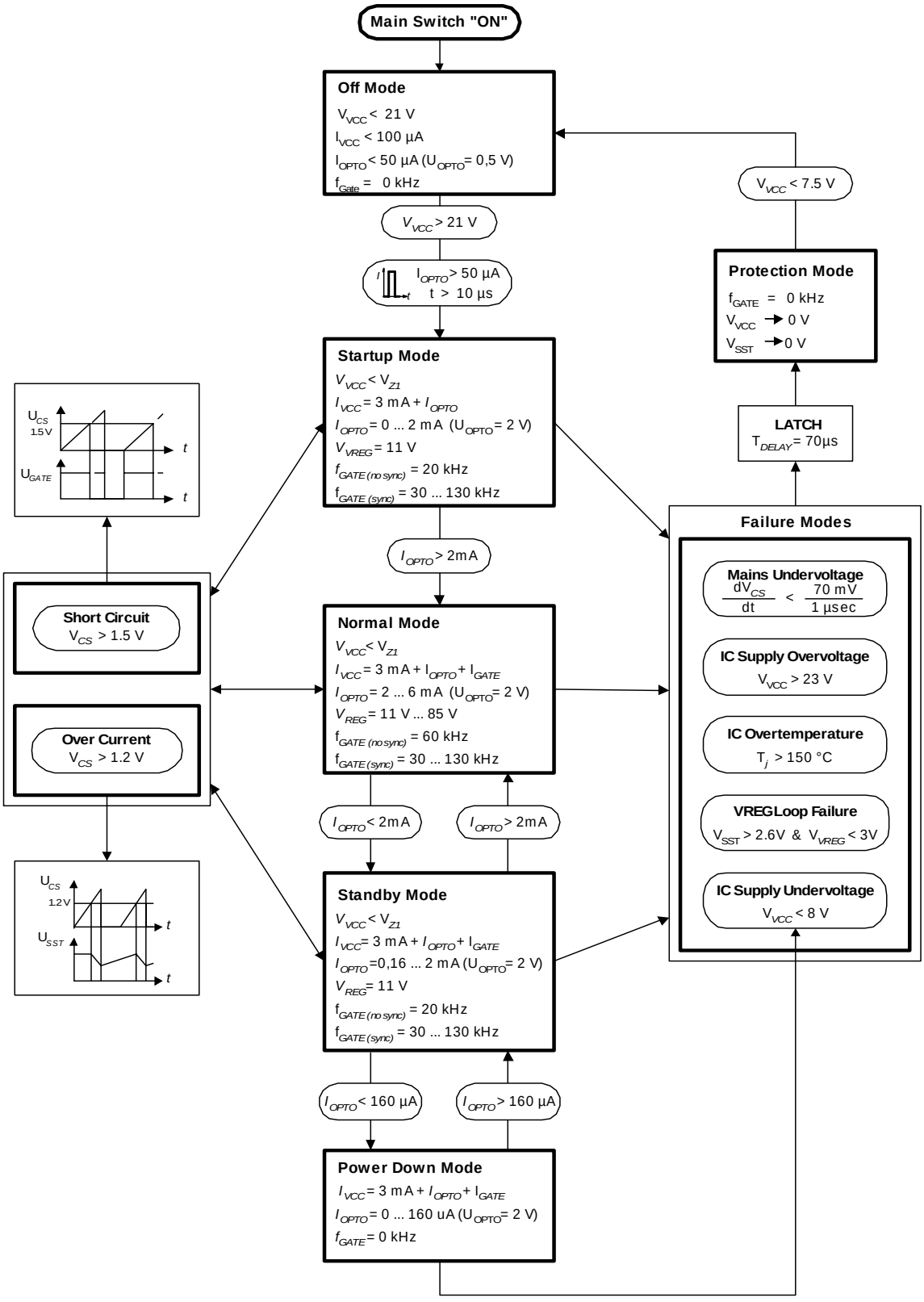


Figure 1 Flow Chart of Operation

Note: If not otherwise stated the figures shown in this section represent typical performance characteristic

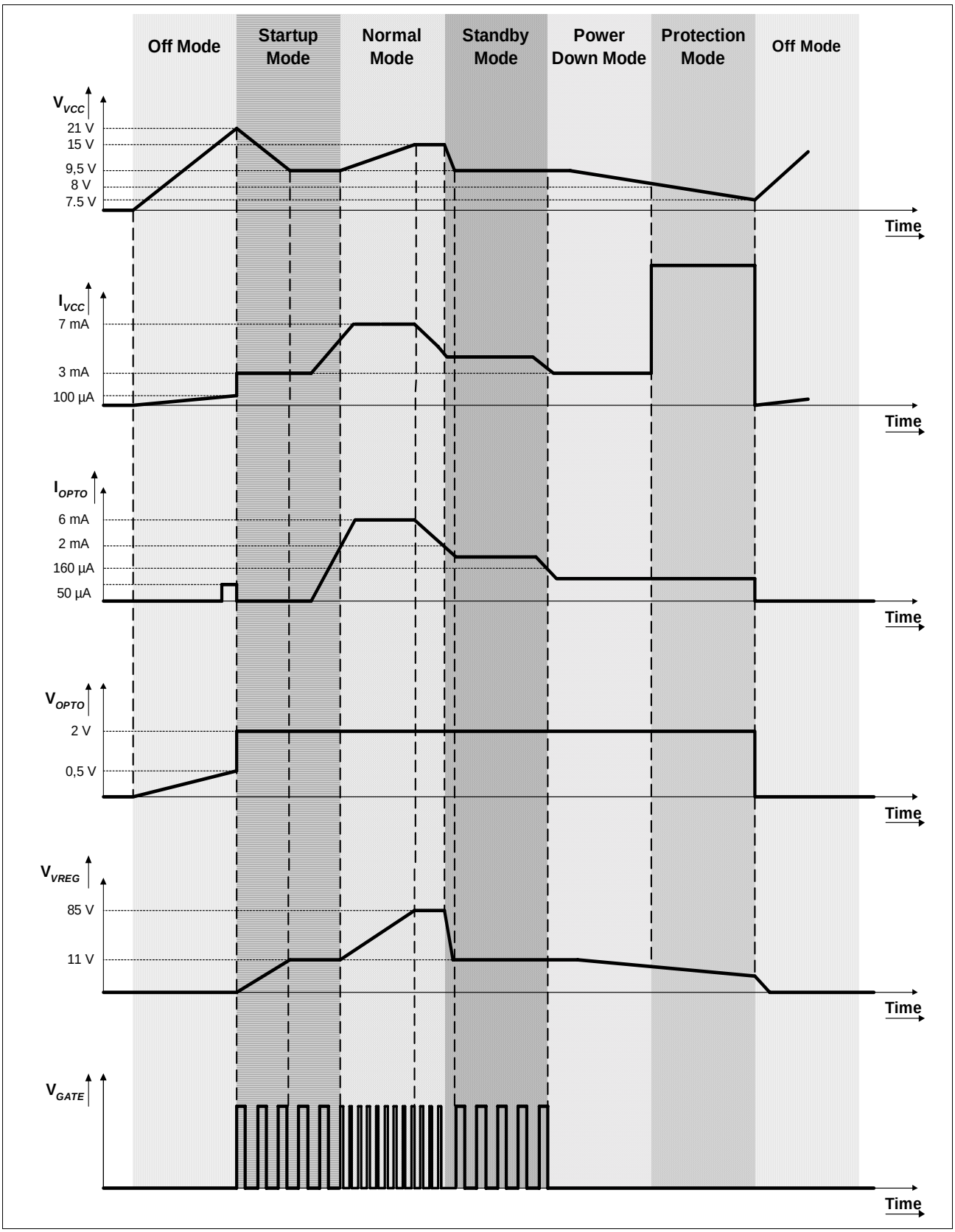


Figure 2 Timing Diagram of Operation without synchronization

(see **Figure 1, Page4** and **Figure 2, Page 5**)

2.1 Off mode / Switch on process

At first the chip is in off mode. During switch on process the supply voltage at VCC increases from 0 V to the switch on threshold of V_{VCC}. The total current consumption of TDA 16850-2 is typ.100 µA in this case. When V_{VCC} exceeds the voltage of 21 V the chip can be activated by an optocoupler current pulse higher than 50 µA (typ.) and 10 µs (typ.) duration.

2.2 Startup Mode

Entering startup mode the internal supply of TDA 16850-2 is switched on and all blocks are operable. In the startup mode a current out of pin OPTO of 0 µA < $|I_{OPTO}|$ < 2 mA is allowed. If there is no signal at pin SYNC, the TDA 16850-2 generates gate pulses at a rate of 20 kHz (typ.). The pulse width is first increased during a soft start and then regulated for 11 V voltage at Pin VREG.

2.3 Normal Mode

Normal mode can be entered from startup mode or standby mode by increasing the opto current above 2 mA (typ.). In the normal mode the supply voltage must be 8 V < V_{VCC} < 23 V typ. When there is no signal present at SYNC, GATE clocks with a frequency of typical f_{OSC} = 60 kHz (typ.). If there is a signal at SYNC of 30 kHz < f_{OSC} < 130kHz the internal oscillator is synchronized automatically with this signal. If the VREG voltage is higher than 11 V, the output pulse width depends on the opto current. A higher opto current means wider output pulses and a higher output power of the power supply. Duty cycle minimum will be achieved at a OPTO current of 2 mA (typ.).

2.4 Standby Mode

Standby mode is reached from either normal mode or power down mode by adjusting the opto current within 160 µA to 2 mA.

Voltage V_{VREG} will then be regulated to typ. 11 V. The Oscillator frequency in standby mode is typ. 20 kHz. A signal at pin SYNC is also evaluated in standby mode and the oscillator is synchronized accordingly.

Standby mode can be quit to move to normal mode, power down mode, or to move to protection mode.

In the standby mode the supply to the chip can be switched over from pin VCC to pin VREG. The switch is a current limiting switching transistor. It's switched on when V_{VCC} drops below typ. 10 V in normal mode. When V_{VREG} is greater than V_{VCC} the chip is now supplied via V_{VREG}. At the same time the internal control of the duty cycle at GATE is set so that there is typically a voltage of 11 V at pin VREG. At VCC there is then a voltage of typ. 9.5 V. The current at pin OPTO must stay between 160 µA < $|I_{OPTO}|$ < 2 mA.

2.5 Power down Mode

At power down mode GATE will be disabled. The power down mode is entered when the OPTO input current is less than 160 µA (typ.), after the IC has been in the normal mode before.

2.6 Protection Mode

All failure modes will disable GATE. This is the protection mode, which is latched and VCC and SST will be discharged by internal transistors. Protection mode can only be left through the off mode if V_{VCC} is below 7.5 V (typ.).

2.7 Protection Circuitry

2.7.1 Over Current

The voltage at pin CS will be sensed by a comparator. Until the voltage at pin CS is more than 1,2V (typ.) the duty cycle will be reduced by discharging Pin SST by a internal transistor.

2.7.2 Short Circuit

In case of a secondary short circuit, GATE will be disabled as long as the voltage at pin CS is more than 1,5 V (typ.).

2.7.3 Failure Modes

The error message of the failure functions are stored in a latch after a delay of typ. 70 µs. GATE then will be disabled. The latch is reset again when the chip is in off mode .

2.7.3.1 Mains Undervoltage

A circuit checks the rise of the ramp singal at pin CS for minimum slew rate.

2.7.3.2 IC Supply Overvoltage

A circuit checks the voltage at pin VCC.

2.7.3.3 IC Overtemperature

A thermal probe checks the temperature of the chip.

2.7.3.4 VREG Loop Failure

A circuit checks if the voltage at VREG is below 3 V (typ.) and the voltage at pin SST have reached 2,6V (typ.).

2.7.3.5 IC SupplyUndervoltage

A comparator checks the voltage at VCC.

3 Functional Block Description

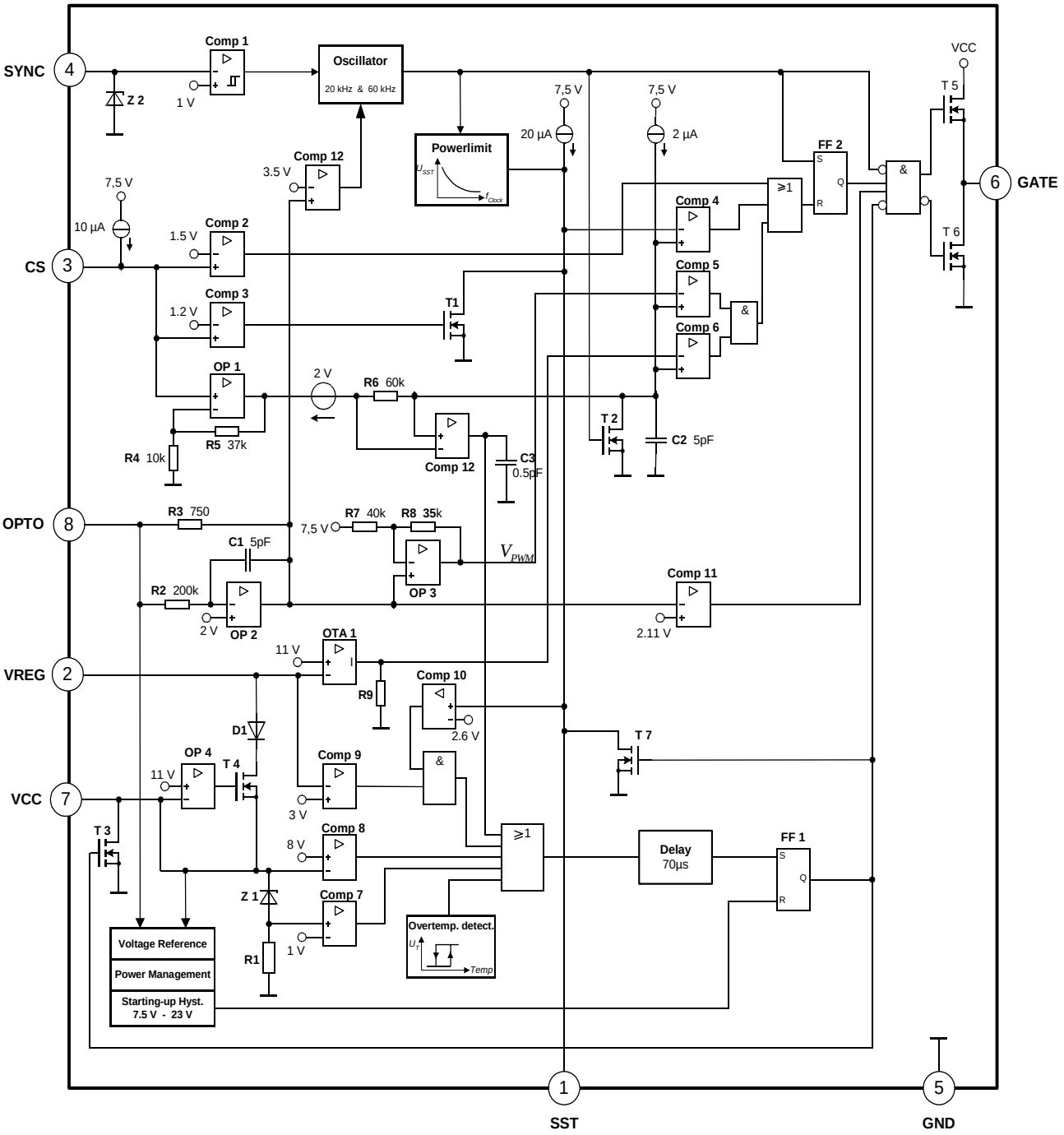


Figure 3 Block Diagram

3.1 VCC and VREG Section

The TDA 16850-2 is protected against overvoltages above 23 V typ. by an internal Zener diode Z1 at pin VCC (see **Figure 4**).

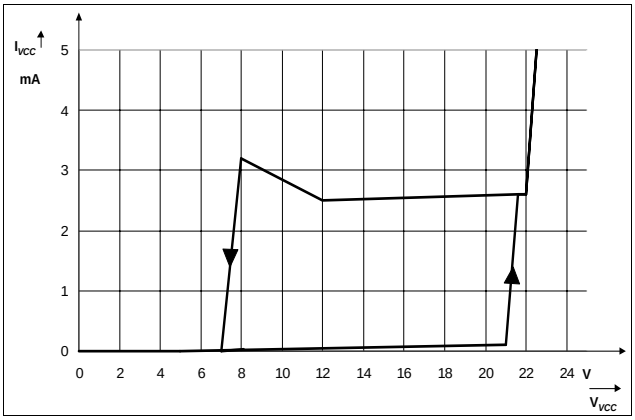


Figure 4 Undervoltage Lockout Hysteresis and Zener Diode Overvoltage Protection

In the normal mode the chip is supplied via VCC. The nominal voltage at VCC then is typ. 15 V. The feedback path leads from a secondary voltage (e.g. 190 V) through a secondary reference element (i.e. TL 431) and the optocoupler to the feedback pin OPTO (see **Figure 19**) .

In standby mode the chip is supplied via pin VREG. Pin VREG is then the feedback input at the same time. The voltage at VREG is regulated to typ. 11 V via **OTA1** (see **Figure 5**). The intern supply voltages are then derived from the voltage at VREG via **OP4**, **D1** and **T4**

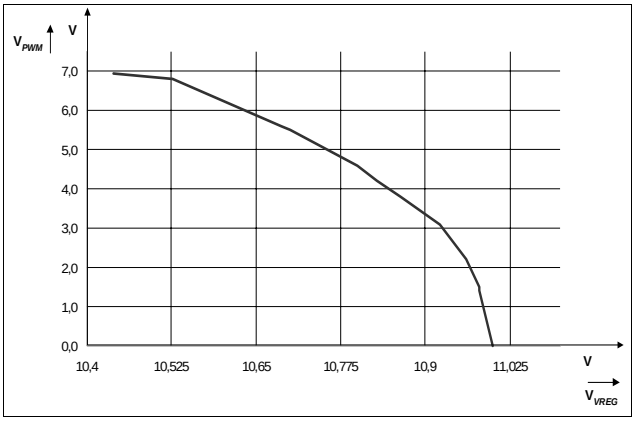


Figure 5 Transferfunction of OTA1

3.2 OPTO Section

At pin OPTO (see **Figure 6**) the TDA 16850-2 has an integrated 150 kHz lowpass filter which eliminates interference spikes .

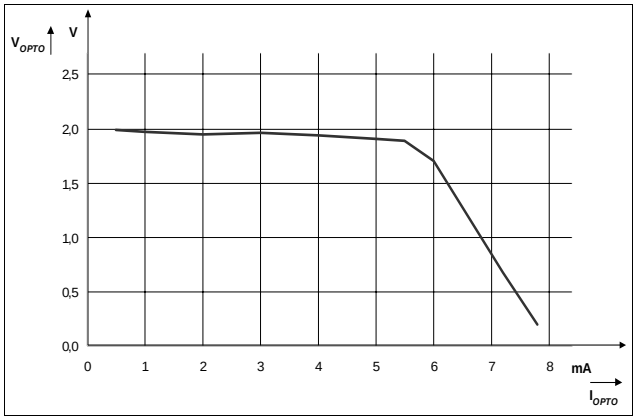


Figure 6 Output Characteristic of Pin OPTO

In normal mode Pin OPTO is the feedback input for the TDA 16850-2 via OP2 (see **Figure 7**).

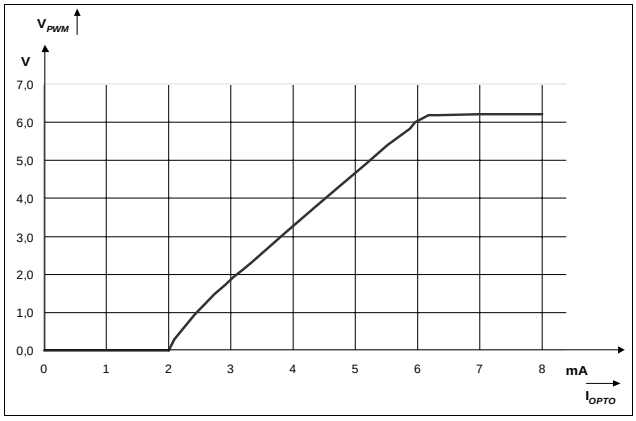


Figure 7 Transferfunction of OP2

Comp11 checks the current at pin OPTO. If I_{OPTO} falls below 160 µA GATE will be disabled .

3.3 Oscillator and Synchronization

In standby mode and in startup mode the oscillator frequency is typ. 20 kHz. In normal mode the unsynchronized oscillator frequency is typ. 60 kHz.

If there is a signal present at SYNC within 30 kHz to 130 kHz, the oscillator switches automatically to synchronized operation.

The Synchronisation input is positive edge triggered. The GATE output pulse begins after the rising edge of

the SYNC signal with a delay, which is 1/20 of the SYNC signal period (see **Figure 8**).

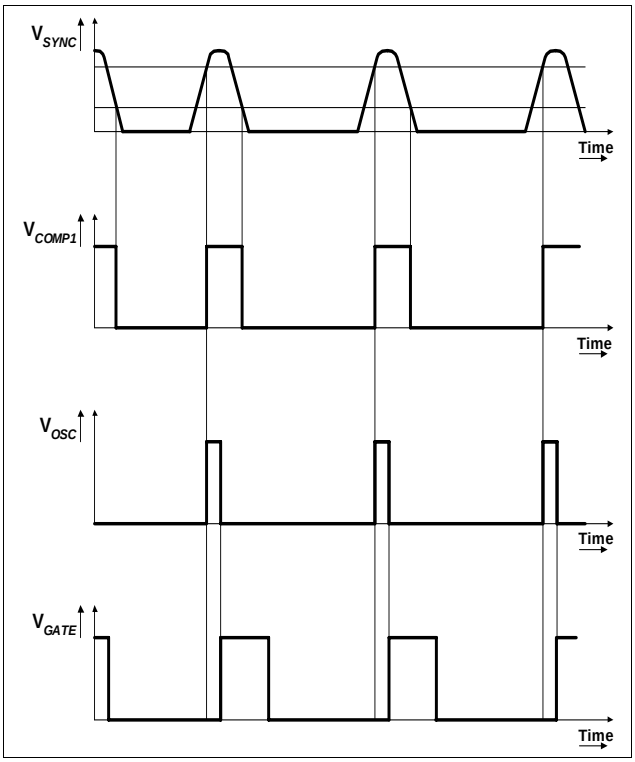


Figure 8 Timing Diagram Oscillator with Synchronisation

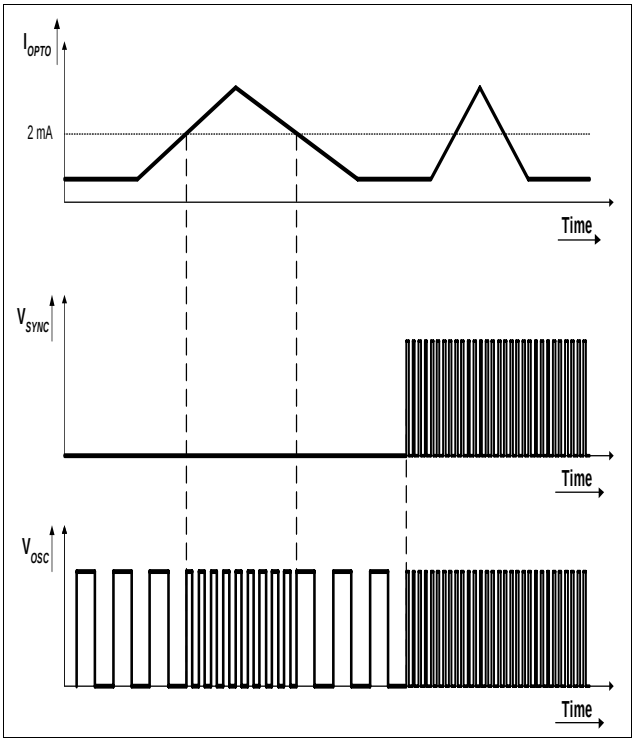


Figure 9 Timing Diagram 60/20 kHz Switch and Synchronisation

If I_{OPTO} falls below 2 mA the unsynchronized oscillator will switch from 60 kHz to 20 kHz (see **Figure 9**).

The sync input is protected by a Zener diode **Z2** and a hysteresis comparator **Comp1**.

3.4 PWM Section

The PWM Section is equipped with improved current mode control.

The pulse width modulator of the TDA 16850-2 operates at a small pulse width in voltage mode and with a larger pulse width in current mode. The GATE puls depends on the SST voltage via **Comp4**, the OPTO current via **Comp5** and the VREG voltage via **Comp6**. A voltage at VREG lower than 11 V will lead to long GATE pulses, as well as a high OPTO current. A low voltage at SST dominates over the OPTO and VREG conditions and sets the limit for the maximum GATE pulse width. The input, which generates the longer GATE pulses will dominate over the input, which would generate the shorter Gate pulses (see **Figure 10**).

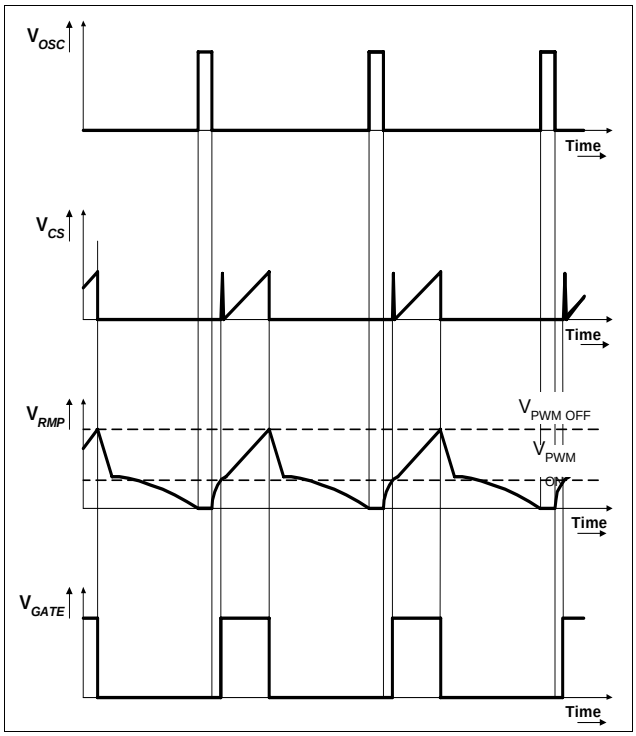


Figure 10 Timing Diagram PWM Section

3.5 Current Sense Section

The voltage at the shunt resistor of the Power MOS is fed to **OP1** (see **Figure 11**) via pin CS. No other external circuit is required. An internal low pass filter with an initial condition suppresses a leading spike at CS up to 150nVs typ.

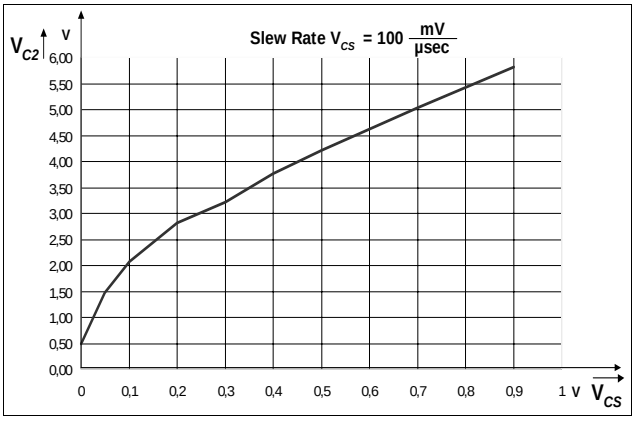


Figure 11 Transferfunction of OP1

3.6 Soft Start

On the transition from off mode to startup mode a soft start is activated. Depending on the voltage at the capacitor at pin SST the increasing of the duty cycle is controlled via **Comp4**.

3.7 Output Power Limiting

After the end of the soft start there is a maximum voltage at the capacitor at pin SST. This voltage is a signal for the maximum possible pulse width at GATE via **Comp4**.

The maximum voltage at SST is regulated depending on the oscillator frequency. The value of the voltage is derived from the square root of the oscillator period. The energy that can be stored in the transformer is reduced in proportion to the oscillator frequency. The maximum output power is idependent from SYNC frequency (see **Figure 12**).This reduces the danger of fire if a defect within the load circuit occurs.

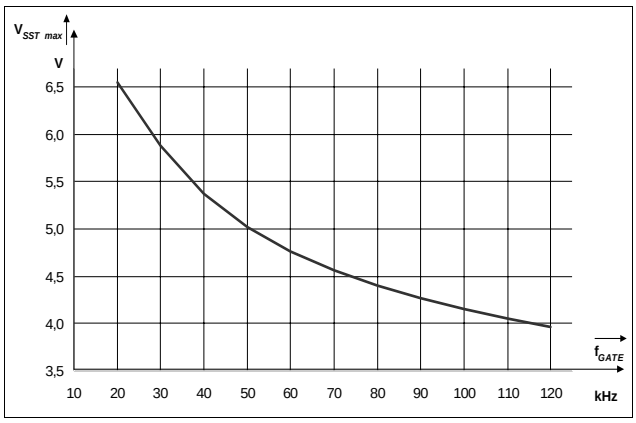


Figure 12 Voltage at Softstart Capacitor vs. Oscillator Frequency

3.8 GATE Driver

GATE switches from low to high first with high current and then with reduced current. This current switchover takes place at a voltage at GATE of typ. 6 V (see **Figure 13**).

In off mode GATE is safely disabled, i.e. low. In this state transients at drain with miller currents up to 20 mA can not open the power MOS.

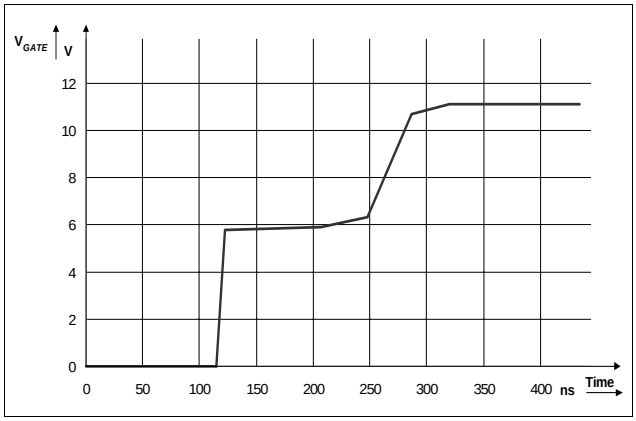


Figure 13 Rising Edge of Driver Output

3.9 Protection Circuitry

3.9.1 Over Current

A slow current limitation is realized with **Comp3**. If the voltage at pin CS reached 1,2V (typ.) pin SST will be discharged by **T1** (see **Figure 14**).

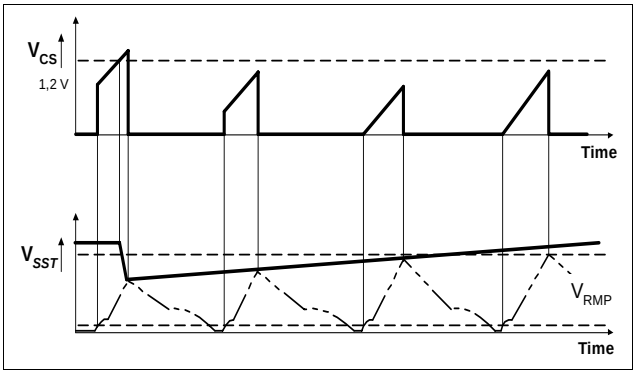


Figure 14 Timing Diagram Over Current Function

3.9.2 Short Circuit

By means of the fast comparator **Comp2** sensing at pin CS peak current limitation is realized. When being activated (V_{CS} > 1,5V typ.) it will immediately shut down the GATE (see **Figure 15**).

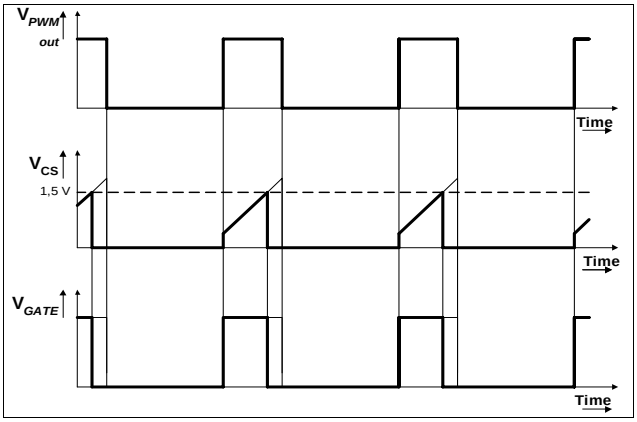


Figure 15 Protection Function Short Circuit

3.9.3 Failure Modes

The failure modes are stored in **FF1** after typically 70µs. GATE then will be disabled und pin SST and VCC discharged by **T7** and **T3. FF1** is reset again when the chip is in off mode (see **Figure 16**).

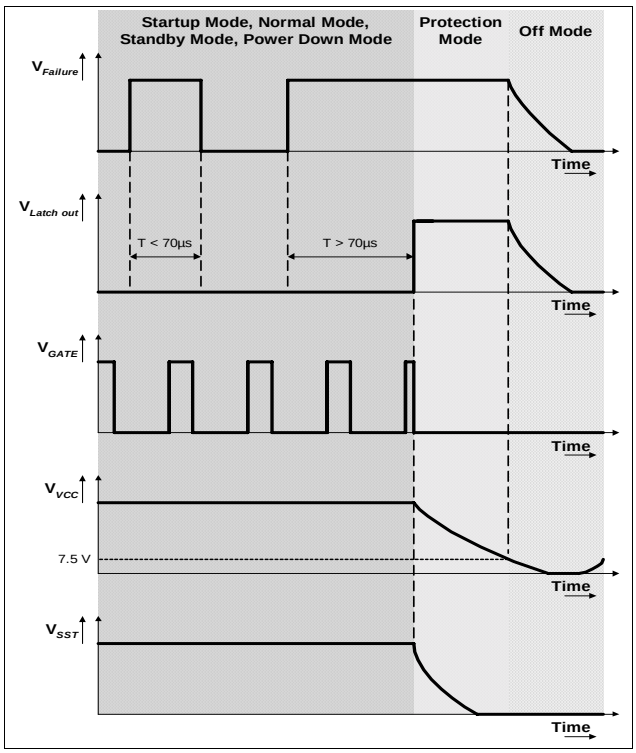


Figure 16 Timing Diagram Failure Mode

3.9.3.1 Mains Undervoltage

Comp12 checks the rise of the ramp signal at pin CS for minimum slew rate. If the ramp rise falls below a lower limit value this means the mains voltage is too low. The GATE output is disabled then.

3.9.3.2 IC Supply Overvoltage

A further Comparator **Comp7** disables GATE, if a current of more than 4 mA typ. flows over the Zener diode **Z1** at VCC, i.e. if there is overvoltage at VCC caused by a loop fault.

3.9.3.3 IC Overtemperature

If in case of an error condition the TDA 16850-2 is supplied over an extended period from a high feed voltage at VREG, the chip will dissipate high power. An internal overtemperature detection disables GATE via **FF1** if there is a thermal overload.

3.9.3.4 VREG Loop Failure

Comp9 and **Comp10** checks the voltage at pin VREG and SST. If V_{VREG} is below 3 V and V_{SST} have reached 2,6V (typ.), i.e. if there is undervoltage at pin VREG caused by a loop fault, GATE will be disabled.

3.9.3.5 IC Supply Undervoltage

Comp8 checks the voltage at pin VCC. If V_{VCC} falls below 8 V GATE will be disabled.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. To avoid destruction make sure, that for any pin except for pin GATE the currents caused by transient processes stay well below 100 mA. For the same reason make sure, that any capacitor that will be connected to pin VCC and pin VREG is discharged before assembling the application circuit.

T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC supply voltage	V_{VCC}	– 0,3	V_{Z1}	V	V_{Z1} = 23 V typ.
VREG supply voltage	V_{VREG}	– 0,3	85	V	-
Zener current of Z1	I_{Z1}	-	10	mA	-
SYNC current	I_{SYNC}	-10	10	mA	V_{SYNC} < – 0,3 V or V_{SYNC} > 5 V
OPTO voltage	V_{OPTO}	– 0,3	8	V	-
SST voltage	V_{SST}	– 0,3	8	V	-
CS voltage	V_{CS}	– 0,3	8	V	-
GATE dc current	I_{GATE}	– 100	100	mA	-
GATE dc peak clamping current	I_{GATE}	-	100	mA	V_{GATE} = High
GATE dc peak clamping current	I_{GATE}	– 500	-	mA	V_{GATE} = Low
GATE charge	Q_{GATE}	– 200	200	nC	each slope, V_{VCC} < 20 V
Junction temperature	T_J	– 25	150	°C	-
Storage temperature	T_S	– 65	150	°C	-
Thermal resistance	R_{thJA}	-	100	K/W	P-DIP-8

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC supply voltage	V_{VCC}	0	V_{Z1}	V	V_{Z1} = Zener voltage of Z1
VREG voltage	V_{VREG}	0	85	V	-
Zener current	I_{Z1}	0	4	mA	Limited by $T_{J,max}$
GATE current	I_{GATE}	– 1	1,5	A	-
GATE dc clamping current	I_{GATE}	–200	50	mA	-
Synchronization range	f_{SYNC}	30	130	kHz	-
Capacitor on SST	C_{SST}	1		nF	-
Junction temperature	T_J	– 25	150	°C	-
SYNC duty cycle	DC	10	90	%	-

4.3 Characteristics

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range T_A from – 25 °C to 85 °C Typical values represent the median values, which are related to production processes. If not otherwise stated, a supply voltage of V_{VCC} = 15 V is assumed..)

Supply Section VCC and VREG

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zener voltage	V_{Z1}	21	23	28	V	I_{Z1}=4mA, I_{OPTO}=0
Quiescent supply current	I_{VCC} or I_{VREG}	5	6	9	mA	GATE disabled I_{OPTO} = 4 mA
		5	7	10	mA	GATE enabled I_{OPTO} = 4 mA C_L = 0
Supply current	I_{VCC} + I_{VREG}	7	11	15	mA	GATE enabled I_{OPTO} = 4 mA C_L = 4,7 nF f_{SYNC} = 100 kHz
Standby regulation voltage via VREG	V_{VREG}	10	11	12	V	V_{GATE}>2V
Switch drop voltage, SW1, from VREG to VCC, closed	V_{SW1}	-	1,4	2,3	V	I_{SW1} = 8 mA V_{VREG} = 10 V
VREG input resistance, from VREG to GND, SW1 opened	R_{VREG}	60	110	180	kΩ	
Off mode, threshold	V_{VCC}	6,5	7,5	8,5	V	
Power up, rising voltage threshold, off mode to startup mode	V_{VCCUP}	19	21	24	V	correlated to V_{Z1} I_{OPTO} = 120 µA
Power up, threshold current, off mode to startup mode	I_{VCCUP}	30	100	170	µA	V_{VCC}=V_{VCCUP} – 0,1V

OPTO Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Static OPTO current, threshold off mode to startup mode	$I_{OPTO\ DC}$	–100	–50	–20	µA	V_{VCC} = V_{VCCUP} + 0,5 V
OPTO current, pulswidth off mode to startup mode	$I_{OPTO\ PULS}$	4	7,5	20	µs	I_{OPTO} = 100µA V_{VCC} = V_{VCCUP} + 0,5 V
OPTO current, threshold startup mode to normal mode	I_{OPTO}	–2500	–2000	–1400	µA	
OPTO current, threshold normal mode to standby mode and back	I_{OPTO}	–2500	–2000	–1400	µA	
OPTO current, threshold standby mode to power down mode and back	I_{OPTO}	–240	–160	–70	µA	

OPTO Section

OPTO current limit	I_{OPTO}	-10,5	-8	-6,5	mA	0 V < V_{OPTO} < 0,5V
OPTO voltage	V_{OPTO}	1	2	2,5	V	200 µA < |I_{OPTO}|< 5 mA
OPTO current for duty cycle minimum	I_{OPTO}	–2600	–2000	-1500	µA	
OPTO current for duty cycle maximum	I_{OPTO}	–6,6	–6	–5,4	mA	correlated to duty cycle minimum

Oscillator Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Standby mode, no SYNC signal	$f_{STANDBY}$	15	20	25	kHz	-
Normal mode, no SYNC signal	f_{NORMAL}	50	60	70	kHz	-
Oscillator frequency, line regulation	Δf_{OUT}	-	0,08	1	%	ΔV_{VCC} = 9 V f = 60 kHz

SYNC Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
SYNC threshold, voltage rising, leading edge triggered	V_{SYNC}	0,9	1	1,1	V	-
SYNC threshold, hysteresis	V_{SYNC}	0,1	0,2	0,5	V	-
SYNC, input current	I_{SYNC}	-	5	40	µA	0 V < V_{SYNC} < 2 V
SYNC, negative clamp voltage	V_{SYNC}	-1	– 0,7	-0,4	V	I_{SYNC} = – 1 mA
SYNC, positive clamp voltage	V_{SYNC}	2,5	3,5	5	V	I_{SYNC} = 1 mA
min. SYNC range	f_{SYNC}	30	-	130	kHz	130 kHz - 200 kHz
max. SYNC range	f_{SYNC}	17	-	200	kHz	
delay SYNC - GATE	$t_{SYNC - GATE}$	0,7	2,5	3,8	µs	f_{OSC} = 30 kHz
delay SYNC - GATE	$t_{SYNC - GATE}$	0,3	1,2	1,8	µs	f_{OSC} = 120 kHz

PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CS input current	I_{CS}	-5	–10	-20	µA	V_{CS} = 1,35 V
CS spike blanking	SB_{CS}	-	0,15	-	µVs	-
SST softstart, charging current	I_2	10	20	30	µA	-
SST softstart, maximum voltage	V_{SSMAX}	3	6	7,5	V	correlated to power limitation

PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
SST voltage at power limitation max.	V_{PLIMAX}	5,0	6,0	7,5	V	f_{OSC} = 30 kHz
SST voltage at power limitation min.	V_{PLIMIN}	3,0	3,8	4,6	V	f_{OSC} = 120 kHz

GATE Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE low voltage	V_{GATE}	0,5	0,85	1,2	V	V_{VCC} = 2 V I_{GATE} = 5 mA
		0,7	1,0	1,5	V	V_{VCC} = 2 V I_{GATE} = 20 mA
		0,05	0,25	0,35	V	I_{GATE} = 50 mA
		– 0,5	–0,25	-0,05	V	I_{GATE} = – 50 mA
GATE high voltage	V_{GATE}	10	11	12	V	V_{VCC} = 16 V C_L= 4,7 nF
		8	9,7	10	V	V_{VCC} = 10 V C_L= 4,7 nF
		7	8	9	V	V_{VCC} = 9 V C_L= 4,7 nF
GATE rise time	t_r	120	210	380	ns	V_{GATE} = 2 V to 8 V C_L = 4,7 nF
		30	50	100	ns	V_{GATE} = 2 V to 4.5 V C_L = 4,7 nF
GATE fall time	t_f	50	80	130	ns	V_{GATE} = 9 V to 2 V C_L = 4,7 nF
GATE current, peak, rising edge	I_{GATE}	– 1	0,4	-	A	C_L = 4,7 nF
GATE current, peak, falling edge	I_{GATE}	-	1,2	2	A	C_L = 4,7 nF
GATE step voltage	V_{GATE}	5	6	7	V	-
GATE charge	Q_{GATE}		150		nC	f_{OSC} = 130 kHz package P-DIP-8

ERROR Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CS slew rate minimum (Mains Undervoltage)	SR_{CS}	15	45	70	mV /µs	I_{OPTO} = 4 mA f_{OSC} = 30 kHz
VCC threshhold voltage (IC Supply Overvoltage)	V_{VCCmax}	21	23	28	V	-
Temperature protection (IC Overtemperature)	T_J	135	145	155	°C	-
VREG min. voltage (VREG Loop Failure)	V_{VREG}	2,3	3	3,3	V	V_{SST} > 2,6V
VSST max. voltage (VREG Loop Failure)	V_{SST}	2,0	2,6	3,1	V	V_{VREG} < 3V
VCC threshhold voltage (IC Supply Undervoltage)	V_{VCCDWN}	7,0	8.0	8,5	V	-
VCC protection mode discharging current	I_1	10	13	20	mA	V_{VCC} = 11V
SST protection mode discharging current	I_3	1	2,5	4	mA	V_{SST} = 5V
Delay time failure latch active	t_{delay}	30	70	110	µs	-
CS threshold voltage (Over current detection)	$V_{CS\ OC}$	1,1	1,2	1,3	V	-
SST discharge current, at over current detection	I_{DISC}	1,5	3	4,5	mA	V_{SST} = 5V V_{CS} = 2V
CS threshold voltage (Short circuit detection)	$V_{CS\ SC}$	1,35	1,5	1,65	V	-

typ. Max. Duty Cycle dependence on Powerlimitation, frequency and CS slew rate (I_{OPTO} = max)

	V_{CS} slew rate = 80 (mV/µs)		V_{CS} slew rate = 100 (mV/µs)		V_{CS} slew rate = 200 (mV/µs)		V_{CS} slew rate = 300 (mV/µs)	
f_{GATE} (kHz)	V_{CS} max (mV)	Duty Cycle (%)	V_{CS} max (mV)	Duty Cycle (%)	V_{CS} max (mV)	Duty Cycle (%)	V_{CS} max (mV)	Duty Cycle (%)
30	910	36	930	28	1030	16	1170	13
60	580	46	600	38	770	23	870	18
120	390	59	400	57	550	36	670	29

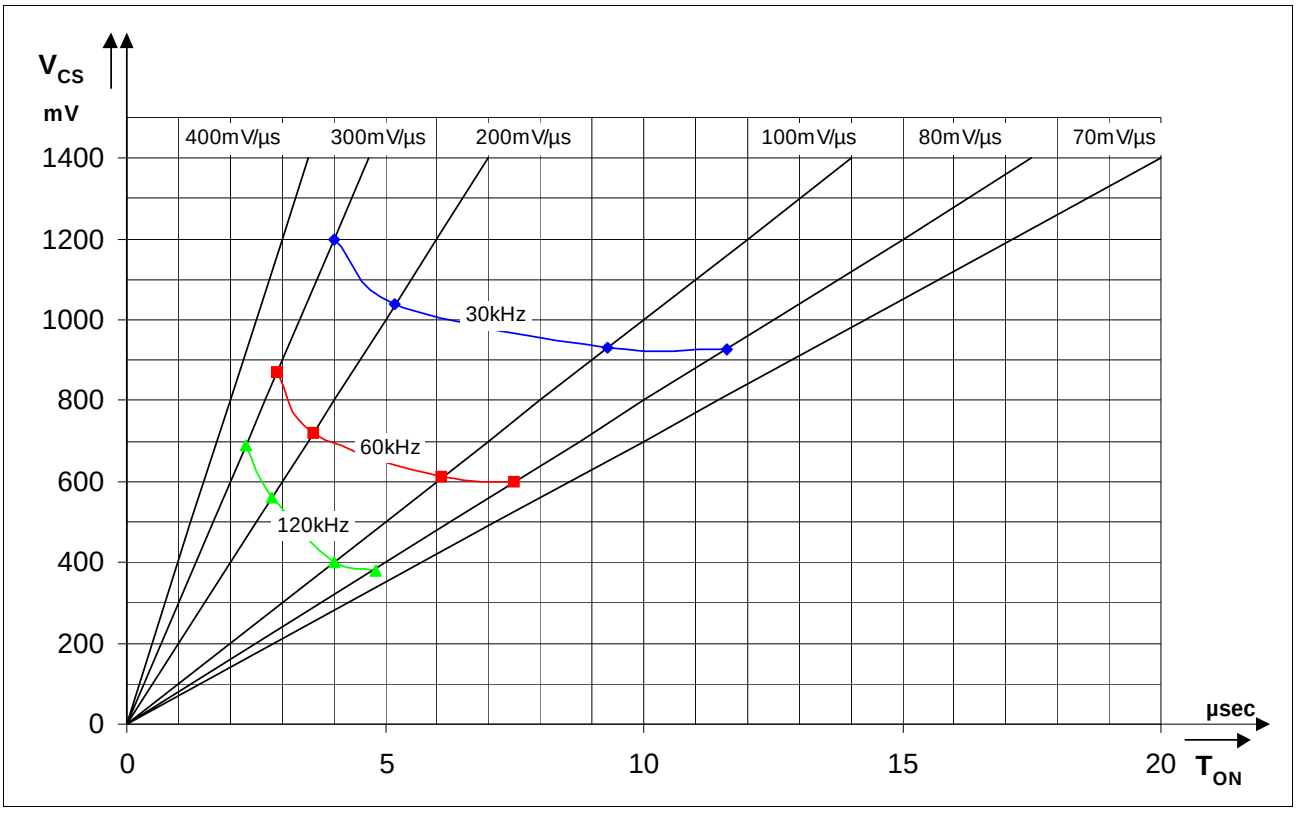


Figure 17

5 Application Circuits

5.1 Application Circuit 1. See Description 5.3.1

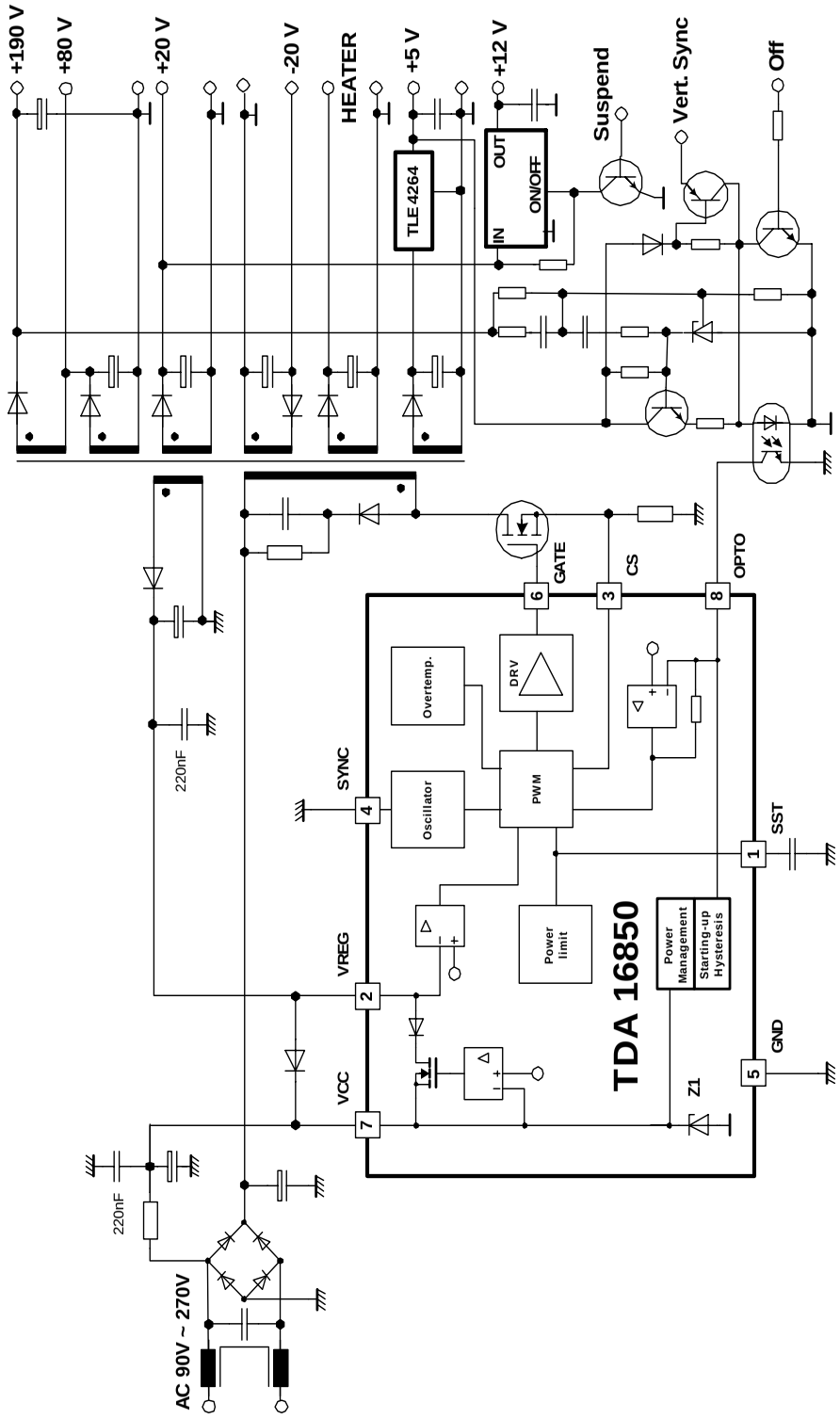


Figure 18

5.2 Application Circuit 2. See Decription 5.3.2

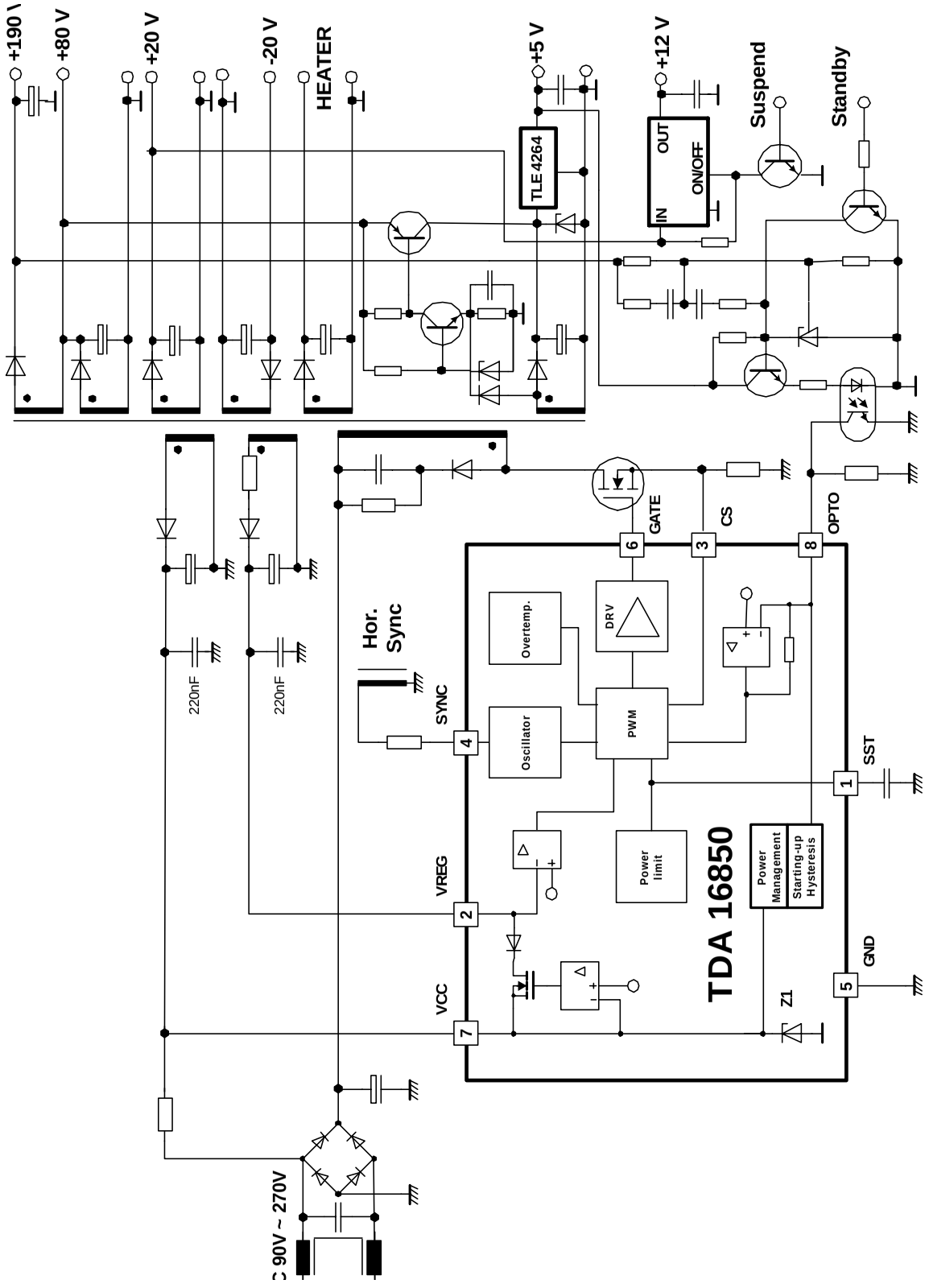


Figure 19

5.3 Description of Application Circuits

The Application Circuits shows two typical Monitor Power Supplies with a wide input voltage range (90 - 230 V AC) and several outputs (+190 V, +80V, +20V, -20V, +12V, Heater, +5V).

5.3.1 Application Circuit 1

Switch on via connector “Vert. Sync”. Switch off via connector “Off”. From off mode to startup mode via “Vert. Sync”. The Power consumption in off mode is less then 1 Watt. This application needs minimal external components.

This application work with 20kHz in startup and standby mode and 60 kHz in normal mode provided by the internal oscillator.

5.3.2 Application Circuit 2

Switch on and switch off via connector “Standby”. No off mode. The 5 V output therefore is always on. Switchover of TLE 4264 input to 80 V winding automatically if the winding voltage becomes too low.
In normal mode the oscialltor is synchronized via pin SYNC.

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