DATA SHEET

TDA4853; TDA4854

I²C-bus autosync deflection controllers for PC/TV monitors

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

I²C-bus autosync deflection controllers for PC/TV monitors

TDA4853; TDA4854

FEATURES

Concept features

- Full horizontal plus vertical autosync capability; TV and VCR mode included
- Extended horizontal frequency range from 15 to 130 kHz
- Comprehensive set of I²C-bus driven geometry adjustments and functions, including standby mode
- Very good vertical linearity
- Moire cancellation
- Start-up and switch-off sequence for safe operation of all power components
- X-ray protection
- Flexible switched mode B+ supply function block for feedback and feed forward converter
- Internally stabilized voltage reference
- Drive signal for focus amplifiers with combined horizontal and vertical parabola waveforms (TDA4854)
- DC controllable inputs for Extremely High Tension (EHT) compensation
- SDIP32 package.

Synchronization

- Can handle all sync signals (horizontal, vertical, composite and sync-on-video)
- Output for video clamping (leading/trailing edge selectable by I²C-bus), vertical blanking and protection blanking
- Output for fast unlock status of horizontal synchronization and blanking on grid 1 of picture tube.

Horizontal section

- I²C-bus controllable wide range linear picture position, pin unbalance and parallelogram correction via horizontal phase
- Frequency-locked loop for smooth catching of horizontal frequency
- TV mode at 15.625 or 15.750 kHz selectable by I²C-bus
- Simple frequency preset of f_{min} and f_{max} by external resistors
- Low jitter
- Soft start for horizontal and B+ control drive signals.

Vertical section

- I²C-bus controllable vertical picture size, picture position, linearity (S-correction) and linearity balance
- Output for I²C-bus controllable vertical sawtooth and parabola (for pin unbalance and parallelogram)
- Vertical picture size independent of frequency
- Differential current outputs for DC coupling to vertical booster.
- 50 to 160 Hz vertical autosync range.

East-West (EW) section

- I²C-bus controllable output for horizontal pincushion, horizontal size, corner and trapezium correction
- Optional tracking of EW drive waveform with line frequency selectable by I²C-bus.

Focus section of TDA4854

- I²C-bus controllable output for horizontal and vertical parabolas
- Vertical parabola is independent of frequency and tracks with vertical adjustments
- Horizontal parabola independent of frequency
- Pre-correction of delay in focus output stage.

GENERAL DESCRIPTION

The TDA4854 is a high performance and efficient solution for autosync monitors. All functions are controllable by I²C-bus.

The TDA4854 provides synchronization processing, horizontal and vertical synchronization with full autosync capability, a TV/VCR mode and very short settling times after mode changes. External power components are given a great deal of protection. The IC generates the drive waveforms for DC-coupled vertical boosters such as the TDA486x and TDA835x.

The TDA4854 provides extended functions e.g. as a flexible B+ control, an extensive set of geometry control facilities, and a combined output for horizontal and vertical focus signals.

The TDA4853 is an economy version of the TDA4854, especially designed for use in 14" and 15" monitors with combined EHT generation. It provides the same features as the TDA4854 except for the dynamic focus block.

Together with the I²C-bus driven Philips TDA488x video processor family, a very advanced system solution is offered.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	9.2	–	16	V
I_{CC}	supply current	–	70	–	mA
$I_{CC(stb)}$	supply current during standby mode	–	9	–	mA
VSIZE	vertical size	60	–	100	%
VGA	VGA overscan for vertical size	–	16.8	–	%
VPOS	vertical position	–	±11.5	–	%
VLIN	vertical linearity (S-correction)	–2	–	–46	%
VLINBAL	vertical linearity balance	–	±2.5	–	%
V_{HSIZE}	horizontal size voltage	0.13	–	3.6	V
V_{HPIN}	horizontal pincushion voltage (EW parabola)	0.04	–	1.42	V
V_{HEHT}	horizontal size modulation voltage	0.02	–	0.69	V
V_{HTRAP}	horizontal trapezium correction voltage	–	±0.33	–	V
V_{HCOR}	horizontal corner correction voltage	–0.64	–	+0.08	V
HPOS	horizontal position	–	±13	–	%
HPARAL	horizontal parallelogram	–	±1	–	%
HPINBAL	EW pin unbalance	–	±1	–	%
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4853	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TDA4854			

BLOCK DIAGRAMS

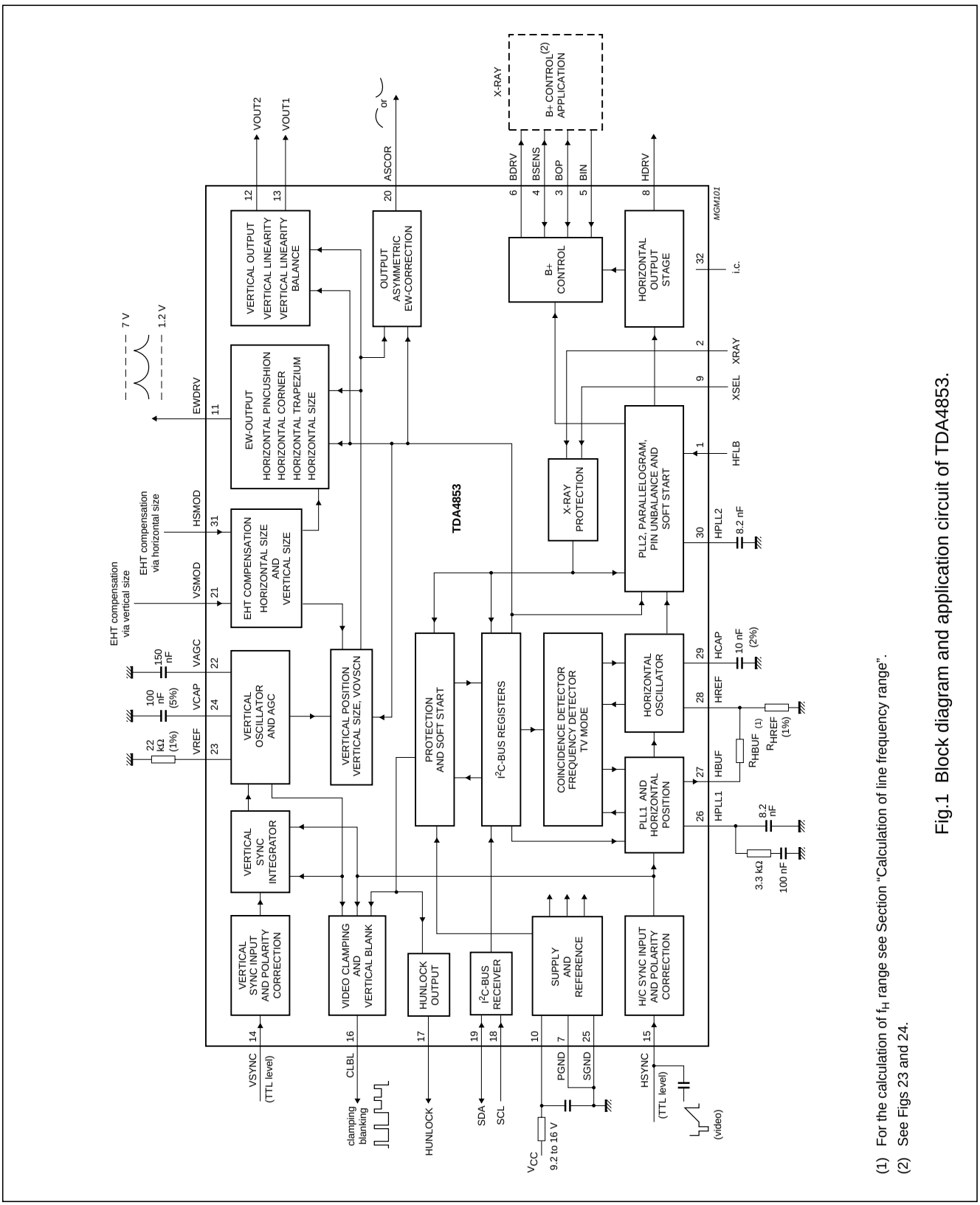


Fig.1 Block diagram and application circuit of TDA4853.

(1) For the calculation of f_H range see Section "Calculation of line frequency range".
(2) See Figs 23 and 24.

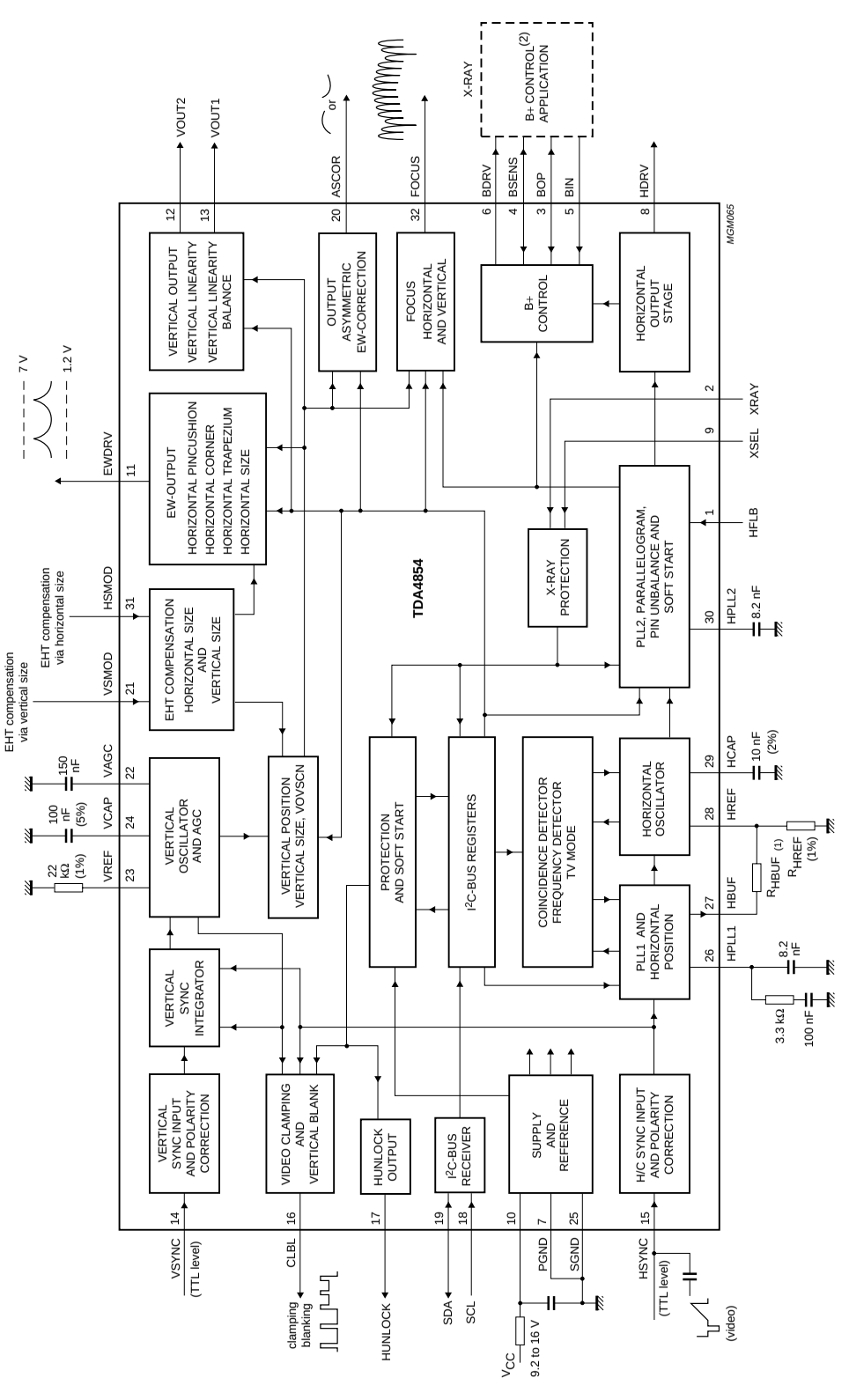


Fig.2 Block diagram and application circuit of TDA4854.

(1) For the calculation of f_H range see Section "Calculation of line frequency range".

(2) See Figs 23 and 24.

PINNING

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output
BSENS	4	B+ control comparator input
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
PGND	7	power ground
HDRV	8	horizontal driver output
XSEL	9	select input for X-ray reset
V_{CC}	10	supply voltage
EWDRV	11	EW waveform output
VOUT2	12	vertical output 2 (ascending sawtooth)
VOUT1	13	vertical output 1 (descending sawtooth)
VSYNC	14	vertical synchronization input
HSYNC	15	horizontal/composite synchronization input
CLBL	16	video clamping pulse/vertical blanking output
HUNLOCK	17	horizontal synchronization unlock/protection/vertical blanking output
SCL	18	I²C-bus clock input
SDA	19	I²C-bus data input/output
ASCOR	20	output for asymmetric EW corrections
VSMOD	21	input for EHT compensation (via vertical size)
VAGC	22	external capacitor for vertical amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
SGND	25	signal ground
HPLL1	26	external filter for PLL1
HBUF	27	buffered f/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HPLL2	30	external filter for PLL2/soft start
HSMOD	31	input for EHT compensation (via horizontal size)
i.c.	32	internally connected; note 1: TDA4853
FOCUS	32	output for horizontal and vertical focus: TDA4854

Note

1. External connections to this pin are not allowed.

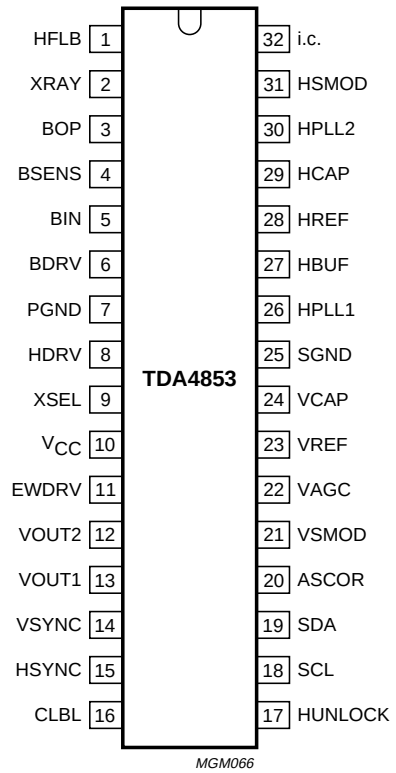


Fig.3 Pin configuration for TDA4853.

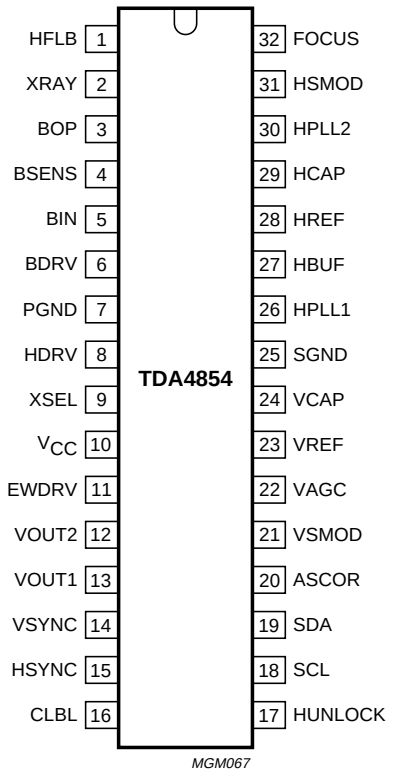


Fig.4 Pin configuration for TDA4854.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

HSYNC (pin 15) is the input for the horizontal synchronization signals, which can be DC-coupled TTL signals (horizontal or composite sync) and AC-coupled negative-going video sync signals. Video syncs are clamped to 1.28 V and sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.

For DC-coupled TTL signals the input clamping current is limited. The slicing level for TTL signals is 1.4 V.

The separated sync signal (either video or TTL) is integrated on an internal capacitor to detect and normalize the sync polarity.

Normalized horizontal sync pulses are used as input signals for the vertical sync integrator, the PLL1 phase detector and the frequency-locked loop.

The presence of equalization pulses is allowed for correct function of the PLL1 phase detector only in TV mode.

Vertical sync integrator

Normalized composite sync signals from HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the horizontal oscillator reference current at HREF (pin 28). The integrator output directly triggers the vertical oscillator.

Vertical sync slicer and polarity correction

Vertical sync signals (TTL) applied to VSYNC (pin 14) are sliced at 1.4 V. The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity. The output signals of vertical sync integrator and sync normalizer are disjuncted before they are fed to the vertical oscillator.

Video clamping/vertical blanking generator

The video clamping/vertical blanking signal at CLBL (pin 16) is a two-level sandcastle pulse which is especially suitable for video ICs such as the TDA488x family, but also for direct applications in video output stages.

The upper level is the video clamping pulse, which is triggered by the horizontal sync pulse. Either the leading or trailing edge can be selected by setting control bit CLAMP via the I²C-bus. The width of the video clamping pulse is determined by an internal single-shot multivibrator.

The lower level of the sandcastle pulse is the vertical blanking pulse, which is derived directly from the internal oscillator waveform. It is started by the vertical sync and stopped with the start of the vertical scan. This results in optimum vertical blanking. Two different vertical blanking times are accessible, by control bit VBLK, via the I²C-bus.

Blanking will be activated continuously if one of the following conditions is true:

- Soft start of horizontal and B+ drive [voltage at HPLL2 (pin 30) pulled down externally or by the I²C-bus]
- PLL1 is unlocked while frequency-locked loop is in search mode or if horizontal sync pulses are absent
- No horizontal flyback pulses at HFLB (pin 1)
- X-ray protection is activated
- Supply voltage at V_{CC} (pin 10) is low (see Fig.25).

Horizontal unlock blanking can be switched off, by control bit BLKDIS, via the I²C-bus while vertical blanking and protection blanking is maintained.

Frequency-locked loop

The frequency-locked loop can lock the horizontal oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and the recommended maximum ratio is $\frac{f_{max}}{f_{min}} = \frac{6.5}{1}$

This can, for instance, be a range from 15.625 to 90 kHz with all tolerances included.

Without a horizontal sync signal the oscillator will be free-running at f_{min}. Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than 4% between horizontal sync and oscillator frequency will switch the horizontal section into search mode. This means that PLL1 control currents are switched off immediately.

The internal frequency detector then starts tuning the oscillator. Very small DC currents at HPLL1 (pin 26) are used to perform this tuning with a well defined change rate. When coincidence between horizontal sync and oscillator frequency is detected, the search mode is first replaced by a soft-lock mode which lasts for the first part of the next vertical period. The soft-lock mode is then replaced by a normal PLL operation. This operation ensures smooth tuning and avoids fast changes of horizontal frequency during catching.

In this concept it is not allowed to load HPLL1.
The frequency dependent voltage at this pin is fed internally to HBUF (pin 27) via a sample-and-hold and buffer stage. The sample-and-hold stage removes all disturbances caused by horizontal sync or composite vertical sync from the buffered voltage. An external resistor connected between pins HBUF and HREF defines the frequency range.

Out-of-lock indication (pin HUNLOCK)

Pin HUNLOCK is floating during search mode if no sync pulses are applied, or if a protection condition is true. All this can be detected by the microcontroller if a pull-up resistor is connected to its own supply voltage.

For an additional fast vertical blanking at grid 1 of the picture tube a 1 V signal referenced to ground is available at this output. The continuous protection blanking (see Section “Video clamping/vertical blanking generator”) is also available at this pin. Horizontal unlock blanking can be switched off, by control bit BLKDIS via the I²C-bus while vertical blanking is maintained.

TV mode

In applications with TV signals the standard frequency-to-voltage converter operation will be disturbed by equalizing sync pulses and phase jumps occurring in VCR signals. To avoid this, a TV mode has been implemented. It can be accessed by choosing the horizontal TV sync frequencies of 15.625 or 15.75 kHz as the minimum frequency for the horizontal oscillator. Applying TV signals will cause the frequency-to-voltage converter to scan down to this frequency in normal operation. If the control bit TVMOD is sent by the I²C-bus, the HBUF output is clamped to 2.5 V and an internally defined PLL1 control range of ±10% is established.
To return to standard operation of the frequency-to-voltage converter the TV bit has to be reset. For an optimal operation with VCR signals the RC combination at pin HPLL1 has to be switched externally.

Horizontal oscillator

The horizontal oscillator is the relaxation type and requires a capacitor of 10 nF to be connected at HCAP (pin 29). For optimum jitter performance the value of 10 nF must not be changed.

The minimum oscillator frequency is determined by a resistor connected between pin HREF and ground. A resistor connected between pins HREF and HBUF defines the frequency range.

The reference current at pin HREF also defines the integration time constant of the vertical sync integration.

Calculation of line frequency range

The oscillator frequencies f_{min} and f_{max} must first be calculated. This is achieved by adding the spread of the relevant components to the highest and lowest sync frequencies $f_{sync(min)}$ and $f_{sync(max)}$. The oscillator is driven by the currents in R_{HREF} and R_{HBUF}.

The following example is a 31.45 to 90 kHz application:

Table 1 Calculation of total spread

spread of	for f_{max}	for f_{min}
IC	±3%	±5%
C_{HCAP}	±2%	±2%
R_{HREF}, R_{HBUF}	±2%	±2%
Total	±7%	±9%

Thus the typical frequency range of the oscillator in this example is:

$$f_{max} = f_{sync\,(max)} \times 1.07 = 96.3\ kHz$$

$$f_{min} = \frac{f_{sync\,(min)}}{1.09} = 28.9\ kHz$$

The TV mode is centred around f_{min} with a control range of ±10%. Activation of the TV mode is only allowed between 15.625 and 35 kHz.

The resistors R_{HREF} and $R_{HBUFpar}$ can be calculated using the following formulae:

$$R_{HREF} = \frac{78 \times kHz \times k\Omega}{f_{min} + 0.0012 \times f_{min}^2\,[kHz]} = 2.61\ k\Omega$$

$$R_{HBUFpar} = \frac{78 \times kHz \times k\Omega}{f_{max} + 0.0012 \times f_{max}^2\,[kHz]} = 726\ \Omega$$

The resistor $R_{HBUFpar}$ is calculated as the value of R_{HREF} and R_{HBUF} in parallel. The formulae for R_{HBUF} also takes into account the voltage swing across this resistor

$$R_{HBUF} = \frac{R_{HREF} \times R_{HBUFpar}}{R_{HREF} - R_{HBUFpar}} \times 0.8 = 805\ \Omega$$

PLL1 phase detector

The phase detector is a standard type using switched current sources, which are independent of the horizontal frequency. It compares the middle of the horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26).

See also Section “Horizontal position adjustment and corrections”.

Horizontal position adjustment and corrections

A linear adjustment of the relative phase between the horizontal sync and the oscillator sawtooth (in PLL1 loop) is achieved via register HPOS. Once adjusted, the relative phase remains constant over the whole frequency range.

Correction of pin unbalance and parallelogram is achieved by modulating the phase between the oscillator sawtooth and horizontal flyback (in loop PLL2) via registers HPARAL and HPINBAL. If those asymmetric EW corrections are performed in the deflection stage, both registers can be disconnected from the horizontal phase via control bit ACD. This does not change the output at pin ASCOR.

Horizontal moire cancellation

To achieve a cancellation of horizontal moire (also known as ‘video moire’), the horizontal frequency is divided-by-two to achieve a modulation of the horizontal phase via PLL2. The amplitude is controlled by register HMOIRE. To avoid a visible structure on screen the polarity changes with half of the vertical frequency. Control bit MOD disables the moire cancellation function.

PLL2 phase detector

The PLL2 phase detector is similar to the PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The control currents are independent of the horizontal frequency. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of the HDRV (pin 8) output pulse.

For the TDA4854 external modulation of the PLL2 phase is not allowed, because this would disturb the start advance of the horizontal focus parabola.

Soft start and standby

If HPLL2 is pulled to ground by resetting the register SOFTST, the horizontal output pulses, vertical output currents and B+ control driver pulses will be inhibited. This means that HDRV (pin 8), BDRV (pin 6), VOUT1 (pin 13) and VOUT2 (pin 12) are floating in this state. If HPLL2 is pulled to ground by an external DC current, vertical output currents stay active while HDRV (pin 8) and BDRV (pin 6) are in floating state. In both cases the PLL2 and the frequency-locked loop are disabled, CLBL (pin 16) provides a continuous blanking signal and HUNLOCK (pin 17) is floating.

This option can be used for soft start, protection and power-down modes. When the HPLL2 pin is released again, an automatic soft start sequence on the horizontal drive as well as on the B+ drive output will be performed (see Figs 26 and 27).

A soft start can only be performed if the supply voltage for the IC is a minimum of 8.6 V.

The soft start timing is determined by the filter capacitor at HPLL2 (pin 30), which is charged with a constant current during soft start. If the voltage at pin 30 (HPLL2) reaches 1.1 V, the vertical output currents are enabled. At 1.7 V the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty cycle is reached. The voltage at HPLL2 increases further and performs a soft start at BDRV (pin 6) as well. The voltage at HPLL2 continues to rise until HPLL2 enters its normal operating range. The internal charge current is now disabled. Finally PLL2 and the frequency-locked loop are activated. If both functions reach normal operation, HUNLOCK (pin 17) switches from the floating status to normal vertical blanking, and continuous blanking at CLBL (pin 16) is removed.

Output stage for line drive pulses [HDRV (pin 8)]

An open-collector output stage allows direct drive of an inverting driver transistor because of a low saturation voltage of 0.3 V at 20 mA. To protect the line deflection transistor, the output stage is disabled (floating) for a low supply voltage at V_{CC} (see Fig.25).

The duty cycle of line drive pulses is slightly dependent on the actual horizontal frequency. This ensures optimum drive conditions over the whole frequency range.

X-ray protection

The X-ray protection input [XRAY (pin 2)] provides a voltage detector with a precise threshold. If the input voltage at XRAY exceeds this threshold level for a certain period of time then control bit SOFTST is reset, which switches the IC into protection mode. In this mode several pins are forced into defined states:

HUNLOCK (pin 17) is floating

The capacitor connected to HPLL2 (pin 30) is discharged

Horizontal output stage (HDRV) is floating

B+ control driver stage (BDRV) is floating

Vertical output stages (VOUT1 and VOUT2) are floating

CLBL provides a continuous blanking signal.

There are two different methods of restarting the IC:

1. XSEL (pin 9) is open-circuit or connected to ground. The control bit SOFTST must be set to logic 1 via the I²C-bus. The IC then returns to normal operation via soft start.
2. XSEL (pin 9) is connected to V_{CC} via an external resistor. The supply voltage of the IC must be switched off for a certain period of time before the IC can be restarted again using the standard power-on procedure.

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of vertical size after changes in sync frequency conditions.

The free-running frequency $f_{fr(V)}$ is determined by the resistor R_{VREF} connected to pin 23 and the capacitor C_{VCAP} connected to pin 24. The value of R_{VREF} is not only optimized for noise and linearity performance in the whole vertical and EW section, but also influences several internal references. Therefore the value of R_{VREF} must not be changed.

Capacitor C_{VCAP} should be used to select the free-running frequency of the vertical oscillator in accordance with the following formula: $f_{fr(V)} = \frac{1}{10.8 \times R_{VREF} \times C_{VCAP}}$

To achieve a stabilized amplitude the free-running frequency $f_{fr(V)}$, without adjustment, should be at least 10% lower than the minimum trigger frequency.
The contributions shown in Table 2 can be assumed.

Table 2 Calculation of $f_{fr(V)}$ total spread

Contributing elements	
Minimum frequency offset between $f_{fr(V)}$ and lowest trigger frequency	10%
Spread of IC	±3%
Spread of R_{VREF}	±1%
Spread of C_{VCAP}	±5%
Total	19%

Result for 50 to 160 Hz application:

$$f_{fr(V)} = \frac{50\ Hz}{1.19} = 42\ Hz$$

The AGC of the vertical oscillator can be disabled by setting control bit AGCDIS via the I²C-bus. A precise external current has to be injected into VCAP (pin 24) to obtain the correct vertical size. This special application mode can be used when the vertical sync pulses are serrated (shifted); this condition is found in some display modes, e.g. when using a 100 Hz upconverter for video signals.

Application hint: VAGC (pin 22) has a high input impedance during scan. Therefore, the pin must not be loaded externally otherwise non-linearities in the vertical output currents may occur due to the changing charge current during scan.

Adjustment of vertical size, VGA overscan and EHT compensation

The amplitude of the differential output currents at VOUT1 and VOUT2 can be adjusted via register VSIZE. Register VOVSCN can activate a +17% step in vertical size for the VGA350 mode.

VSMOD (pin 21) can be used for a DC controlled EHT compensation of vertical size by correcting the differential output currents at VOUT1 and VOUT2. The EW waveforms, (vertical focus), pin unbalance and parallelogram corrections are not affected by VSMOD.

The adjustments for vertical size and vertical position also affect the waveforms of the horizontal pincushion, vertical linearity (S-correction), vertical linearity balance, focus parabola, pin unbalance and parallelogram correction. The result of this interaction is that no re-adjustment of these parameters is necessary after an adjustment of vertical picture size or position.

Adjustment of vertical position, vertical linearity and vertical linearity balance

Register VPOS provides a DC shift at the sawtooth outputs VOUT1 and VOUT2 (pins 13 and 12) and the EW drive output EWDRV (pin 11) in such a way that the whole picture moves vertically while maintaining the correct geometry.

Register VLIN is used to adjust the amount of vertical S-correction in the output signal. This function can be switched off by control bit VSC.

Register VLINBAL is used to correct the unbalance of the vertical S-correction in the output signal. This function can be switched off by control bit VLC.

Adjustment of vertical moire cancellation

To achieve a cancellation of vertical moire (also known as ‘scan moire’) the vertical picture position can be modulated by half the vertical frequency. The amplitude of the modulation is controlled by register VMOIRE and can be switched off via control bit MOD.

Horizontal pincushion (including horizontal size, corner correction and trapezium correction)

EWDRV (pin 11) provides a complete EW drive waveform. The components horizontal pincushion, horizontal size, corner correction and trapezium correction are controlled by the registers HPIN, HSIZE, HCOR and HTRAP. HTRAP can be set to zero by control bit VPC.

The pincushion (EW parabola) amplitude, corner and trapezium correction track with the vertical picture size (VSIZE) and also with the adjustment for vertical picture position (VPOS). The corner correction does not track with the horizontal pincushion (HPIN).

Further the horizontal pincushion amplitude, corner and trapezium correction track with the horizontal picture size, which is adjusted via register HSIZE and the analog modulation input HSMOD.

If the DC component in the EWDRV output signal is increased via HSIZE or I_{HSMOD}, the pincushion, corner and trapezium component of the EWDRV output will be reduced by a factor of $1 - \frac{V_{HSIZE} + V_{HEHT}\left(1 - \frac{V_{HSIZE}}{14.4\ V}\right)}{14.4}$

The value 14.4 V is a virtual voltage for calculation only. The output pin can not reach this value, but the gain (and DC bias) of the external application should be such that the horizontal deflection is reduced to zero when EWDRV reaches 14.4 V.

HSMOD can be used for a DC controlled EHT compensation by correcting horizontal size, horizontal pincushion, corner and trapezium. The control range at this pin tracks with the actual value of HSIZE. For an increasing DC component V_{HSIZE} in the EWDRV output signal, the DC component V_{HEHT} caused by I_{HSMOD} will be reduced by a factor of $1 - \frac{V_{HSIZE}}{14.4\ V}$ as shown in the equation above.

The whole EWDRV voltage is calculated as follows:
$V_{EWDRV} = 1.2\ V + [V_{HSIZE} + V_{HEHT} \times f(HSIZE) + (V_{HPIN} + V_{HCOR} + V_{HTRAP}) \times g(HSIZE, HSMOD)] \times h(I_{HREF})$

Where:

$$V_{HEHT} = \frac{I_{HSMOD}}{120\ \mu A} \times 0.69$$

$$f(HSIZE) = 1 - \frac{V_{HSIZE}}{14.4\ V}$$

$$g(HSIZE, HSMOD) = 1 - \frac{V_{HSIZE} + V_{HEHT}\left(1 - \frac{V_{HSIZE}}{14.4\ V}\right)}{14.4\ V}$$

$$h(I_{HREF}) = \frac{I_{HREF}}{I_{HREF}|_{f = 70kHz}}$$

Two different modes of operation can be chosen for the EW output waveform via control bit FHMULT:

1. Mode 1

   Horizontal size is controlled via register HSIZE and causes a DC shift at the EWDRV output. The complete waveform is also multiplied internally by a signal proportional to the line frequency [which is detected via the current at HREF (pin 28)]. This mode is to be used for driving EW diode modulator stages which require a voltage proportional to the line frequency.

2. Mode 2

   The EW drive waveform does not track with the line frequency. This mode is to be used for driving EW modulators which require a voltage independent of the line frequency.

Output stage for asymmetric correction waveforms [ASCOR (pin 20)]

This output is designed as a voltage output for superimposed waveforms of vertical parabola and sawtooth. The amplitude and polarity of both signals can be changed via registers HPARAL and HPINBAL.

Application hint: The TDA4854 offers two possibilities to control registers HPINBAL and HPARAL.

1. Control bit ACD = 1

   The two registers now control the horizontal phase by means of internal modulation of the PLL2 horizontal phase control. The ASCOR output (pin 20) can be left unused, but it will always provide an output signal because the ASCOR output stage is not influenced by the control bit ACD.

2. Control bit ACD = 0.

   The internal modulation via PLL2 is disconnected. In order to obtain the required effect on the screen, pin ASCOR must now be fed to the DC amplifier which controls the DC shift of the horizontal deflection. This option is useful for applications which already use a DC shift transformer.

If the tube does not need HPINBAL and HPARAL, then pin ASCOR can be used for other purposes, i.e. for a simple dynamic convergence.

TDA4854: dynamic focus section [FOCUS (pin 32)]

This section generates a complete drive signal for dynamic focus applications. The amplitude of the horizontal parabola is internally stabilized, thus it is independent of the horizontal frequency. The amplitude can be adjusted via register HFOCUS. Changing horizontal size may require a correction of HFOCUS. To compensate for the delay in external focus amplifiers a 'pre-correction' for the phase of the horizontal parabola has been implemented. The amplitude of the vertical parabola is independent of frequency and tracks with all vertical adjustments. The amplitude can be adjusted via register VFOCUS. FOCUS (pin 32) is designed as a voltage output for the superimposed vertical and horizontal parabolas.

B+ control function block

The B+ control function block of the TDA4853; TDA4854 consists of an Operational Transconductance Amplifier (OTA), a voltage comparator, a flip-flop and a discharge circuit. This configuration allows easy applications for different B+ control concepts. See also Application Note AN96052: *"B+ converter Topologies for Horizontal Deflection and EHT with TDA4855/58"*.

GENERAL DESCRIPTION

The non-inverting input of the OTA is connected internally to a high precision reference voltage. The inverting input is connected to BIN (pin 5). An internal clamping circuit limits the maximum positive output voltage of the OTA. The output itself is connected to BOP (pin 3) and to the inverting input of the voltage comparator. The non-inverting input of the voltage comparator can be accessed via BSENS (pin 4).

B+ drive pulses are generated by an internal flip-flop and fed to BDRV (pin 6) via an open-collector output stage. This flip-flop is set at the rising edge of the signal at HDRV (pin 8). The falling edge of the output signal at BDRV has a defined delay of $t_{d(BDRV)}$ to the rising edge of the HDRV pulse (see Fig.21). When the voltage at BSENS exceeds the voltage at BOP, the voltage comparator output resets the flip-flop and, therefore, the open-collector stage at BDRV is floating again.

An internal discharge circuit allows a well defined discharge of capacitors at BSENS. BDRV is active at a LOW-level output voltage (see Figs 23 and 24), thus it requires an external inverting driver stage.

The B+ function block can be used for B+ deflection modulators in many different ways. Two popular application combinations are as follows:

- Boost converter in feedback mode (see Fig.23)

  In this application the OTA is used as an error amplifier with a limited output voltage range. The flip-flop is set on the rising edge of the signal at HDRV. A reset will be generated when the voltage at BSENS, taken from the current sense resistor, exceeds the voltage at BOP.

  If no reset is generated within a line period. The rising edge of the next HDRV pulse forces the flip-flop to reset. The flip-flop is set immediately after the voltage at BSENS has dropped below the threshold voltage $V_{RESTART(BSENS)}$.
- Buck converter in feed forward mode (see Fig.24)

  This application uses an external RC combination at BSENS to provide a pulse width which is independent from the horizontal frequency. The capacitor is charged via an external resistor and discharged by the internal discharge circuit. For normal operation the discharge circuit is activated when the flip-flop is reset by the internal voltage comparator. The capacitor will now be discharged with a constant current until the internally controlled stop level $V_{STOP(BSENS)}$ is reached. This level will be maintained until the rising edge of the next HDRV pulse sets the flip-flop again and disables the discharge circuit.

  If no reset is generated within a line period, the rising edge of the next HDRV pulse automatically starts the discharge sequence and resets the flip-flop. When the voltage at BSENS reaches the threshold voltage $V_{RESTART(BSENS)}$, the discharge circuit will be disabled automatically and the flip-flop will be set immediately. This behaviour allows a definition of the maximum duty cycle of the B+ control drive pulse by the relationship of charge current to discharge current.

Supply voltage stabilizer, references, start-up procedures and protection functions

The TDA4853; TDA4854 provides an internal supply voltage stabilizer for excellent stabilization of all internal references. An internal gap reference, especially designed for low-noise, is the reference for the internal horizontal and vertical supply voltages. All internal reference currents and drive current for the vertical output stage are derived from this voltage via external resistors.

If either the supply voltage is below 8.3 V or no data from the I²C-bus has been received after power-up, the internal soft start and protection functions do not allow any of those outputs [HDRV, BDRV, VOUT1, VOUT2 and HUNLOCK (see Fig.25)] to be active.

For supply voltages below 8.3 V the internal I²C-bus will not generate an acknowledge and the IC is in standby mode. This is because the internal protection circuit has generated a reset signal for the soft start register (SOFTST). Above 8.3 V data is accepted and all registers can be loaded. If the SOFTST register has received a set from the I²C-bus, the internal soft start procedure is released, which activates all above mentioned outputs.

If during normal operation the supply voltages has dropped below 8.1 V, the protection mode is activated and HUNLOCK (pin 17) changes to the protection status and is floating. This can be detected by the microcontroller.

This protection mode has been implemented in order to protect the deflection stages and the picture tube during start-up, shut-down and fault conditions. This protection mode can be activated as shown in Table 3.

Table 3 Activation of protection mode

ACTIVATION	RESET
Low supply voltage at pin 10	increase supply voltage; reload registers; soft start via I²C-bus
Power dip, below 8.1 V	reload registers; soft start via I²C-bus
X-ray protection (pin 2) triggered, XSEL (pin 9) is open-circuit or connected to ground	reload registers; soft start via I²C-bus
X-ray protection (pin 2) triggered, XSEL (pin 9) connected to V_{CC} via an external resistor	switch V_{CC} off and on again, reload registers; soft start via I²C-bus
HPLL2 (pin 30) externally pulled to ground	release pin 30

When the protection mode is active, several pins of the TDA4853; TDA4854 are forced into a defined state:

HDRV (horizontal driver output) is floating

BDRV (B+ control driver output) is floating

HUNLOCK (indicates, that the frequency-to-voltage converter is out of lock) is floating (HIGH via external pull-up resistor)

CLBL provides a continuous blanking signal

VOUT1 and VOUT2 (vertical outputs) are floating

The capacitor at HPLL2 is discharged.

If the soft start procedure is activated via the I²C-bus, all of these actions will be performed in a well defined sequence (see Figs 25 and 26).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages measured with respect to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+16	V
$V_{i(n)}$	input voltage for pins:				
	BIN		–0.5	+6.0	V
	HSYNC, VSYNC, VREF, HREF, VSMOD and HSMOD		–0.5	+6.5	V
	SDA and SCL		–0.5	+8.0	V
	XRAY		–0.5	+8.0	V
$V_{o(n)}$	output voltage for pins:				
	VOUT2, VOUT1 and HUNLOCK		–0.5	+6.5	V
	BDRV and HDRV		–0.5	+16	V
$V_{I/O(n)}$	input/output voltages at pins BOP and BSENS		–0.5	+6.0	V
$I_{o(HDRV)}$	horizontal driver output current		–	100	mA
$I_{i(HFLB)}$	horizontal flyback input current		–10	+10	mA
$I_{o(CLBL)}$	video clamping pulse/vertical blanking output current		–	–10	mA
$I_{o(BOP)}$	B+ control OTA output current		–	1	mA
$I_{o(BDRV)}$	B+ control driver output current		–	50	mA
$I_{o(EWDRV)}$	EW driver output current		–	–5	mA
$I_{o(FOCUS)}$	focus driver output current		–	–5	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{ESD}	electrostatic discharge for all pins	note 1	–150	+150	V
		note 2	–2000	+2000	V

Notes

1. Machine model: 200 pF; 0.75 μH; 10 Ω.
2. Human body model: 100 pF; 7.5 μH; 1500 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	K/W

QUALITY SPECIFICATION

In accordance with *"URF-4-2-59/601"*; EMC emission/immunity test in accordance with *"DIS 1000 4.6"* (IEC 801.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EMC}	emission test	note 1	–	1.5	–	mV
	immunity test	note 1	–	2.0	–	V

Note

1. Tests are performed with application reference board. Tests with other boards will have different results.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; peripheral components in accordance with Figs 1 and 2; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal sync separator						
INPUT CHARACTERISTICS FOR DC-COUPLED TTL SIGNALS: HSYNC (PIN 15)						
$V_{i(HSYNC)}$	sync input signal voltage		1.7	–	–	V
$V_{HSYNC(sl)}$	slicing voltage level		1.2	1.4	1.6	V
$t_{r(HSYNC)}$	rise time of sync pulse		10	–	500	ns
$t_{f(HSYNC)}$	fall time of sync pulse		10	–	500	ns
$t_{W(HSYNC)(min)}$	minimum width of sync pulse		0.7	–	–	µs
$I_{i(HSYNC)}$	input current	V_{HSYNC} = 0.8 V	–	–	–200	µA
		V_{HSYNC} = 5.5 V	–	–	10	µA
INPUT CHARACTERISTICS FOR AC-COUPLED VIDEO SIGNALS (SYNC-ON-VIDEO, NEGATIVE SYNC POLARITY)						
V_{HSYNC}	sync amplitude of video input signal voltage	R_{source} = 50 Ω	–	300	–	mV
$V_{HSYNC(sl)}$	slicing voltage level (measured from top sync)	R_{source} = 50 Ω	90	120	150	mV
$V_{clamp(HSYNC)}$	top sync clamping voltage level	R_{source} = 50 Ω	1.1	1.28	1.5	V
$I_{ch(HSYNC)}$	charge current for coupling capacitor	$V_{HSYNC} > V_{clamp(HSYNC)}$	1.7	2.4	3.4	µA
$t_{W(HSYNC)(min)}$	minimum width of sync pulse		0.7	–	–	µs
$R_{source(max)}$	maximum source resistance	duty cycle = 7%	–	–	1500	Ω
$R_{i(diff)(HSYNC)}$	differential input resistance	during sync	–	80	–	Ω
Automatic polarity correction for horizontal sync						
$\frac{t_{P(H)}}{t_H}$	horizontal sync pulse width related to t_H		–	–	25	%
$t_{d(HPOL)}$	delay time for changing polarity		0.3	–	1.8	ms
Vertical sync integrator						
$t_{int(V)}$	integration time for generation of a vertical trigger pulse	f_H = 15.625 kHz; I_{HREF} = 0.52 mA	14	20	26	µs
		f_H = 31.45 kHz; I_{HREF} = 1.052 mA	7	10	13	µs
		f_H = 64 kHz; I_{HREF} = 2.141 mA	3.9	5.7	6.5	µs
		f_H = 100 kHz; I_{HREF} = 3.345 mA	2.5	3.8	4.5	µs
Vertical sync slicer (DC-coupled, TTL compatible): VSYNC (pin 14)						
$V_{i(VSYNC)}$	sync input signal voltage		1.7	–	–	V
$V_{VSYNC(sl)}$	slicing voltage level		1.2	1.4	1.6	V
$I_{i(VSYNC)}$	input current	0 V < V_{SYNC} < 5.5 V	–	–	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic polarity correction for vertical sync						
$t_{VSYNC(max)}$	maximum width of vertical sync pulse		–	–	400	µs
$t_{d(VPOL)}$	delay time for changing polarity		0.45	–	1.8	ms
Video clamping/vertical blanking output: CLBL (pin 16)						
$t_{clamp(CLBL)}$	width of video clamping pulse	measured at V_{CLBL} = 3 V	0.6	0.7	0.8	µs
$V_{clamp(CLBL)}$	top voltage level of video clamping pulse		4.32	4.75	5.23	V
TC_{clamp}	temperature coefficient of $V_{clamp(CLBL)}$		–	4	–	mV/K
$STPS_{clamp}$	steepness of slopes for clamping pulse	R_L = 1 MΩ; C_L = 20 pF	–	50	–	ns/V
$t_{d(HSYNCt-CLBL)}$	delay between trailing edge of horizontal sync and start of video clamping pulse	clamping pulse triggered on trailing edge of horizontal sync; control bit CLAMP = 0; measured at V_{CLBL} = 3 V	–	130	–	ns
$t_{clamp(max)}$	maximum duration of video clamping pulse referenced to end of horizontal sync		–	–	1.0	µs
$t_{d(HSYNCl-CLBL)}$	delay between leading edge of horizontal sync and start of video clamping pulse	clamping pulse triggered on leading edge of horizontal sync; control bit CLAMP = 1; measured at V_{CLBL} = 3 V	–	300	–	ns
$t_{clamp(max)}$	maximum duration of video clamping pulse referenced to end of horizontal sync		–	–	0.15	µs
$V_{blank(CLBL)}$	top voltage level of vertical blanking pulse	notes 1 and 2	1.7	1.9	2.1	V
$t_{blank(CLBL)}$	width of vertical blanking pulse at pins CLBL and HUNLOCK	control bit VBLK = 0	220	260	300	µs
		control bit VBLK = 1	305	350	395	µs
TC_{blank}	temperature coefficient of $V_{blank(CLBL)}$		–	2	–	mV/K
$V_{scan(CLBL)}$	output voltage during vertical scan	I_{CLBL} = 0	0.59	0.63	0.67	V
TC_{scan}	temperature coefficient of $V_{scan(CLBL)}$		–	–2	–	mV/K
$I_{sink(CLBL)}$	internal sink current		2.4	–	–	mA
$I_{L(CLBL)}$	external load current		–	–	–3.0	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal oscillator: HCAP (pin 29) and HREF (pin 28)						
$f_{fr(H)}$	free-running frequency without PLL1 action (for testing only)	$R_{HBUF} = \infty$; $R_{HREF} = 2.4\ k\Omega$; $C_{HCAP} = 10$ nF; note 3	30.53	31.45	32.39	kHz
$\Delta f_{fr(H)}$	spread of free-running frequency (excluding spread of external components)		–	–	±3.0	%
TC_{fr}	temperature coefficient of free-running frequency		–100	0	+100	10^{-6}/K
$f_{H(max)}$	maximum oscillator frequency		–	–	130	kHz
V_{HREF}	voltage at input for reference current		2.43	2.55	2.68	V
Unlock blanking detection: HUNLOCK (pin 17)						
$V_{scan(HUNLOCK)}$	low level voltage of HUNLOCK	saturation voltage in case of locked PLL1; internal sink current = 1 mA	–	–	250	mV
$V_{blank(HUNLOCK)}$	blanking level of HUNLOCK	external load current = 0	0.9	1	1.1	V
TC_{blank}	temperature coefficient of $V_{blank(HUNLOCK)}$		–	–0.9	–	mV/K
TC_{sink}	temperature coefficient of $I_{sink(HUNLOCK)}$		–	0.15	–	%/K
$I_{sink(int)}$	internal sink current	for blanking pulses; PLL1 locked	1.4	2.0	2.6	mA
$I_{L(max)}$	maximum external load current	$V_{HUNLOCK} = 1$ V	–	–	–2	mA
I_{LI}	leakage current	$V_{HUNLOCK} = 5$ V in case of unlocked PLL1 and/or protection active	–	–	±5	µA
PLL1 phase comparator and frequency-locked loop: HPLL1 (pin 26) and HBUF (pin 27)						
$t_{W(HSYNC)(max)}$	maximum width of horizontal sync pulse (referenced to line period)		–	–	25	%
$t_{lock(HPLL1)}$	total lock-in time of PLL1		–	40	80	ms
$I_{ctrl(HPLL1)}$	control currents	notes 4 and 5				
		locked mode, level 1	–	15	–	µA
		locked mode, level 2	–	145	–	µA
V_{HBUF}	buffered f/v voltage at HBUF (pin 27)	minimum horizontal frequency	–	2.5	–	V
		maximum horizontal frequency	–	0.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase adjustments and corrections via PLL1 and PLL2						
HPOS	horizontal position (referenced to horizontal period)	register HPOS = 0	–	–13	–	%
		register HPOS = 127	–	0	–	%
		register HPOS = 255	–	13	–	%
HPINBAL	horizontal pin unbalance correction via HPLL2 (referenced to horizontal period)	register HPINBAL = 0; control bit HPC = 0; note 7	–	–0.8	–	%
		register HPINBAL = 15; control bit HPC = 0; note 7	–	0.8	–	%
		register HPINBAL = X; control bit HPC = 1; note 7	–	0	–	%
HPARAL	horizontal parallelogram correction (referenced to horizontal period)	register HPARAL = 0; control bit HBC = 0; note 7	–	–0.8	–	%
		register HPARAL = 15; control bit HBC = 0; note 7	–	0.8	–	%
		register HPARAL = X; control bit HBC = 1; note 7	–	0	–	%
HMOIRE	relative modulation of horizontal position by ½ horizontal frequency; phase alternates with ½ vertical frequency	register HMOIRE = 0; control bit MOD = 0	–	0	–	%
		register HMOIRE = 31; control bit MOD = 0	–	0.05	–	%
	moire cancellation off	control bit MOD = 1	–	0	–	%
PLL2 phase detector: HFLB (pin 1) and HPLL2 (pin 30)						
ϕ_{PLL2}	PLL2 control (advance of horizontal drive with respect to middle of horizontal flyback)	maximum advance; register HPINBAL = 07; register HPARAL = 07	36	–	–	%
		minimum advance; register HPINBAL = 07; register HPARAL = 07	–	7	–	%
$I_{ctrl(PLL2)}$	PLL2 control current		–	75	–	µA
Φ_{PLL2}	relative sensitivity of PLL2 phase shift related to horizontal period		–	28	–	mV/%
$V_{PROT(PLL2)(max)}$	maximum voltage for PLL2 protection mode/soft start		–	4.4	–	V
$I_{ch(PLL2)}$	charge current for external capacitor during soft start	V_{HPLL2} < 3.7 V	–	1	–	µA
HORIZONTAL FLYBACK INPUT: HFLB (PIN 1)						
$V_{pos(HFLB)}$	positive clamping voltage	I_{HFLB} = 5 mA	–	5.5	–	V
$V_{neg(HFLB)}$	negative clamping voltage	I_{HFLB} = –1 mA	–	–0.75	–	V
$I_{pos(HFLB)}$	positive clamping current		–	–	6	mA
$I_{neg(HFLB)}$	negative clamping current		–	–	–2	mA
$V_{sl(HFLB)}$	slicing level		–	2.8	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output stage for line driver pulses: HDRV (pin 8)						
OPEN-COLLECTOR OUTPUT STAGE						
$V_{sat(HDRV)}$	saturation voltage	I_{HDRV} = 20 mA	–	–	0.3	V
		I_{HDRV} = 60 mA	–	–	0.8	V
$I_{LO(HDRV)}$	output leakage current	V_{HDRV} = 16 V	–	–	10	µA
AUTOMATIC VARIATION OF DUTY CYCLE						
$t_{HDRV(OFF)}/t_H$	relative t_{OFF} time of HDRV output; measured at V_{HDRV} = 3 V; HDRV duty cycle is modulated by the relation I_{HREF}/I_{VREF}	I_{HDRV} = 20 mA; f_H = 31.45 kHz; see Fig.16	42	45	48	%
		I_{HDRV} = 20 mA; f_H = 58 kHz; see Fig.16	45.5	48.5	51.5	%
		I_{HDRV} = 20 mA; f_H = 110 kHz; see Fig.16	49	52	55	%
X-ray protection [XRAY and XSEL (pins 2 and 9)]						
$V_{XRAY(sl)}$	slicing voltage level for latch		6.22	6.39	6.56	V
$t_{W(XRAY)(min)}$	minimum width of trigger pulse		–	–	30	µs
$R_{i(XRAY)}$	input resistance at pin 2	$V_{XRAY} < 6.38\ V + V_{BE}$	500	–	–	kΩ
		$V_{XRAY} > 6.38\ V + V_{BE}$	–	5	–	kΩ
		standby mode	–	5	–	kΩ
$XRAY_{rst}$	reset of X-ray latch	pin 9 open-circuit or connected to GND	set control bit SOFTST via the I²C-bus			–
		pin 9 connected to V_{CC} via R_{XSEL}	switch off V_{CC} then re-apply V_{CC}			–
$V_{CC(XRAY)(min)}$	minimum supply voltage for correct function of the X-ray latch	pin 9 connected to V_{CC} via R_{XSEL}	–	–	4	V
$V_{CC(XRAY)(max)}$	maximum supply voltage for reset of the X-ray latch	pin 9 connected to V_{CC} via R_{XSEL}	2	–	–	V
R_{XSEL}	external resistor at pin 9	no reset via I²C-bus	56	–	130	kΩ
Vertical oscillator [oscillator frequency in application without adjustment of free-running frequency $f_{fr(V)}$]						
$f_{fr(V)}$	free-running frequency	R_{VREF} = 22 kΩ; C_{VCAP} = 100 nF	40	42	43.3	Hz
$f_{cr(V)}$	vertical frequency catching range	constant amplitude; note 8	50	–	160	Hz
V_{VREF}	voltage at reference input for vertical oscillator		–	3.0	–	V
$t_{d(scan)}$	delay between trigger pulse and start of ramp at VCAP (pin 24) (width of vertical blanking pulse)	control bit VBLK = 0	220	260	300	µs
		control bit VBLK = 1	305	350	395	µs
I_{VAGC}	amplitude control current	control bit AGCDIS = 0	±120	±200	±300	µA
		control bit AGCDIS = 1	–	0	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{VAGC}	external capacitor at VAGC (pin 22)		150	–	220	nF
Differential vertical current outputs						
ADJUSTMENT OF VERTICAL SIZE INCLUDING VGA AND EHT COMPENSATION (see Figs 5 to 8)						
VSIZE	vertical size without VGA overscan (referenced to nominal vertical size)	register VSIZE = 0; bit VOVSCN = 0; note 6	–	60	–	%
		register VSIZE = 127; bit VOVSCN = 0; note 6	–	100	–	%
$VSIZE_{VGA}$	vertical size with VGA overscan (referenced to nominal vertical size)	register VSIZE = 0; bit VOVSCN = 1; note 6	–	70	–	%
		register VSIZE = 127; bit VOVSCN = 1; note 6	115.9	116.8	117.7	%
$VSMOD_{EHT}$	EHT compensation on vertical size via VSMOD (pin 21) (referenced to 100% vertical size)	I_{VSMOD} = 0	–	0	–	%
		I_{VSMOD} = –120 µA	–	–7	–	%
$I_{i(VSMOD)}$	input current (pin 21)	VSMOD = 0	–	0	–	µA
		VSMOD = –7%	–	–120	–	µA
$R_{i(VSMOD)}$	input resistance		300	–	500	Ω
$V_{ref(VSMOD)}$	reference voltage at input		–	5.0	–	V
$f_{ro(VSMOD)}$	roll-off frequency (–3 dB)	I_{VSMOD} = –60 µA + 15 µA (RMS)	1	–	–	MHz
ADJUSTMENT OF VERTICAL POSITION (see Figs 5 to 11)						
VPOS	vertical position (referenced to 100% vertical size)	register VPOS = 0; control bit VPC = 0	–	–11.5	–	%
		register VPOS = 127; control bit VPC = 0	–	11.5	–	%
		register VPOS = X; control bit VPC = 1	–	0	–	%
ADJUSTMENT OF VERTICAL LINEARITY (see Figs 5 to 11)						
VLIN	vertical linearity (S-correction)	register VLIN = 0; control bit VSC = 0; note 6	–	2	–	%
		register VLIN = 15; control bit VSC = 0; note 6	–	46	–	%
		register VLIN = X; control bit VSC = 1; note 6	–	0	–	%
δVLIN	symmetry error of S-correction	maximum VLIN	–	–	±0.7	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADJUSTMENT OF VERTICAL LINEARITY BALANCE (see Figs 5 to 11)						
VLINBAL	vertical linearity balance (referenced to 100% vertical size)	register VLINBAL = 0; control bit VLC = 0; note 6	–3.3	–2.5	–1.7	%
		register VLINBAL = 15; control bit VLC = 0; note 6	1.7	2.5	3.3	%
		register VLINBAL = X; control bit VLC = 1; note 6	–	0	–	%
VMOIRE	modulation of vertical picture position by ½ vertical frequency (related to 100% vertical size)	register VMOIRE = 0; control bit MOD = 0	–	0	–	%
		register VMOIRE = 31; control bit MOD = 0	–	0.08	–	%
	moire cancellation off	control bit MOD = 1	–	0	–	%
Vertical output stage: VOUT1 (pin 13) and VOUT2 (pin 12); see Fig.29						
$\Delta I_{VOUT(nom)(p-p)}$	nominal differential output current (peak-to-peak value)	$\Delta I_{VOUT} = I_{VOUT1} - I_{VOUT2}$; nominal settings; note 6	0.76	0.85	0.94	mA
$I_{o(VOUT)(max)}$	maximum output current at pins VOUT1 and VOUT2	control bit VOVSCN = 1	0.54	0.6	0.66	mA
V_{VOUT}	allowed voltage at outputs		0	–	4.2	V
$\delta I_{os(vert)(max)}$	maximum offset error of vertical output currents	nominal settings; note 6	–	–	±2.5	%
$\delta I_{lin(vert)(max)}$	maximum linearity error of vertical output currents	nominal settings; note 6	–	–	±1.5	%
EW drive output						
EW DRIVE OUTPUT STAGE: EWDRV (PIN 11) (see Figs 9 to 12)						
$V_{const(EWDRV)}$	bottom output voltage at pin EWDRV (internally stabilized)	register HPIN = 0; register HCOR = 04; register HTRAP = 08; register HSIZE = 255	1.05	1.2	1.35	V
$V_{o(EWDRV)(max)}$	maximum output voltage	note 9	7.0	–	–	V
$I_{L(EWDRV)}$	load current		–	–	±2	mA
TC_{EWDRV}	temperature coefficient of output signal		–	–	600	10^{-6}/K
$V_{HPIN(EWDRV)}$	horizontal pincushion voltage	register HPIN = 0; note 6	–	0.04	–	V
		register HPIN = 63; note 6	–	1.42	–	V
$V_{HCOR(EWDRV)}$	horizontal corner correction voltage	register HCOR = 0; control bit VSC = 0; note 6	–	0.08	–	V
		register HCOR = 31; control bit VSC = 0; note 6	–	–0.64	–	V
		register HCOR = X; control bit VSC = 1; note 6	–	0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{HTRAP(EWDRV)}$	horizontal trapezium correction voltage	register HTRAP = 15; control bit VPC = 0; note 6	–	–0.33	–	V
		register HTRAP = 0; control bit VPC = 0; note 6	–	0.33	–	V
		register HTRAP = X; control bit VPC = 1; note 6	–	0	–	V
$V_{HSIZE(EWDRV)}$	horizontal size voltage	register HSIZE = 255; note 6	–	0.13	–	V
		register HSIZE = 0; note 6	–	3.6	–	V
$V_{HEHT(EWDRV)}$	EHT compensation on horizontal size via HSMOD (pin 31)	I_{HSMOD} = 0; note 6	–	0.69	–	V
		I_{HSMOD} = –120 μA; note 6	–	0.02	–	V
$I_{i(HSMOD)}$	input current (pin 31)	V_{HEHT} = 0.02 V	–	0	–	μA
		V_{HEHT} = 0.69 V	–	–120	–	μA
$R_{i(HSMOD)}$	input resistance		300	–	500	Ω
$V_{ref(HSMOD)}$	reference voltage at input	I_{HSMOD} = 0	–	5.0	–	V
$f_{ro(HSMOD)}$	roll-off frequency (–3 dB)	I_{HSMOD} = –60 μA + 15 μA (RMS)	1	–	–	MHz
TRACKING OF EWDRV OUTPUT SIGNAL WITH f_H PROPORTIONAL VOLTAGE						
$f_{H(MULTI)}$	horizontal frequency range for tracking		15	–	80	kHz
$V_{PAR(EWDRV)}$	parabola amplitude at EWDRV (pin 11)	I_{HREF} = 1.052 mA; f_H = 31.45 kHz; control bit FHMULT = 1; note 10	–	0.72	–	V
		I_{HREF} = 2.341 mA; f_H = 70 kHz; control bit FHMULT = 1; note 10	–	1.42	–	V
		function disabled; control bit FHMULT = 0; note 10	–	1.42	–	V
LE_{EWDRV}	linearity error of horizontal frequency tracking		–	–	8	%
Output for asymmetric EW corrections: ASCOR (pin 20)						
$V_{HPARAL(ASCOR)}$	vertical sawtooth voltage for EW parallelogram correction	register HPARAL = 0; control bit HPC = 0; note 6	–	–0.825	–	V
		register HPARAL = 15; control bit HPC = 0; note 6	–	0.825	–	V
		register HPARAL = X; control bit HPC = 1; note 6	–	0.05	–	V
$V_{HPINBAL(ASCOR)}$	vertical parabola voltage for pin unbalance correction	register HPINBAL = 0; control bit HBC = 0; note 6	–	–1.0	–	V
		register HPINBAL = 15; control bit HBC = 0; note 6	–	1.0	–	V
		register HPINBAL = X; control bit HBC = 1; note 6	–	0.05	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(ASCOR)(max)(p-p)}$	maximum output voltage swing (peak-to-peak value)		–	4	–	V
$V_{o(ASCOR)(max)}$	maximum output voltage		–	6.5	–	V
$V_{c(ASCOR)}$	centre voltage		–	4.0	–	V
$V_{o(ASCOR)(min)}$	minimum output voltage		–	1.9	–	V
$I_{o(ASCOR)(max)}$	maximum output current	$V_{ASCOR} \geq 1.9$ V	–	–1.5	–	mA
$I_{sink(ASCOR)(max)}$	maximum output sink current	$V_{ASCOR} \geq 1.9$ V	–	50	–	µA
Focus section: FOCUS (pin 32); TDA4854 only						
$V_{HFOCUS(p-p)}$	amplitude of horizontal parabola (peak-to-peak value)	register HFOCUS = 0	–	0.06	–	V
		register HFOCUS = 31	–	3.2	–	V
t_{precor}	pre-correction of phase	1.9 µs < t_{fb} < 5.5 µs	–	350	–	ns
$t_{(W)hfb(min)}$	minimum horizontal flyback pulse width	typical t_{precor} = 350 ns	1.9	–	–	µs
$t_{(W)hfb(max)}$	maximum horizontal flyback pulse width	typical t_{precor} = 350 ns	–	–	5.5	µs
$t_{(W)hfb(TV)(max)}$	maximum horizontal flyback pulse width (TV)	typical t_d = 300 ns	–	–	12.5	µs
$V_{VFOCUS(p-p)}$	amplitude of vertical parabola (peak-to-peak value)	register VFOCUS = 0; note 6	–	0.02	–	V
		register VFOCUS = 07; note 6	–	0.8	–	V
$V_{o(FOCUS)(max)}$	maximum output voltage	I_{FOCUS} = 0	5.7	6	6.3	V
$V_{o(FOCUS)(min)}$	minimum output voltage	I_{FOCUS} = 0	1.7	2	2.3	V
$I_{o(FOCUS)(max)}$	maximum output current		±1.5	–	–	mA
$C_{L(FOCUS)}$	maximum capacitive load		–	–	20	pF
B+ control section (see Figs 23 and 24)						
TRANSCONDUCTANCE AMPLIFIER: BIN (PIN 5) AND BOP (PIN 3)						
$V_{i(BIN)}$	input voltage pin 5		0	–	5.25	V
$I_{i(BIN)(max)}$	maximum input current pin 5		–	–	±1	µA
$V_{ref(int)}$	reference voltage at internal non-inverting input of OTA		2.37	2.5	2.58	V
$V_{o(BOP)(min)}$	minimum output voltage pin 3		–	–	0.5	V
$V_{o(BOP)(max)}$	maximum output voltage pin 3	I_{BOP} < 1 mA	5.0	5.3	5.6	V
$I_{o(BOP)(max)}$	maximum output current pin 3		–	±500	–	µA
$g_{m(OTA)}$	transconductance of OTA	note 11	30	50	70	mS
$G_{v(ol)}$	open-loop voltage gain	note 12	–	86	–	dB
$C_{BOP(min)}$	minimum value of capacitor at pin 3		10	–	–	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VOLTAGE COMPARATOR: BSENS (PIN 4)						
$V_{i(BSENS)}$	voltage range of positive comparator input		0	–	5	V
$V_{i(BOP)}$	voltage range of negative comparator input		0	–	5	V
$I_{LI(BSENS)(max)}$	maximum leakage current	discharge disabled	–	–	–2	µA
OPEN-COLLECTOR OUTPUT STAGE: BDRV (PIN 6)						
$I_{o(BDRV)(max)}$	maximum output current		20	–	–	mA
$I_{LO(BDRV)}$	output leakage current	V_{BDRV} = 16 V	–	–	3	µA
$V_{sat(BDRV)}$	saturation voltage	I_{BDRV} < 20 mA	–	–	300	mV
$t_{off(BDRV)(min)}$	minimum off-time		–	250	–	ns
$t_{d(BDRV-HDRV)}$	delay between BDRV pulse and HDRV pulse	measured at $V_{HDRV} = V_{BDRV}$ = 3 V	–	500	–	ns
BSENS DISCHARGE CIRCUIT (PIN 4)						
$V_{STOP(BSENS)}$	discharge stop level	capacitive load; I_{BSENS} = 0.5 mA	0.85	1.0	1.15	V
$I_{dch(BSENS)}$	discharge current	V_{BSENS} > 2.5 V	4.5	6.0	7.5	mA
$V_{th(BSENS)(restart)}$	threshold voltage for restart	fault condition	1.2	1.3	1.4	V
$C_{BSENS(min)}$	minimum value of capacitor at pin 4		2	–	–	nF
Internal reference, supply voltage, soft start and protection						
$V_{CC(stab)}$	external supply voltage for complete stabilization of all internal references		9.2	–	16	V
I_{CC}	supply current		–	70	–	mA
$I_{CC(stb)}$	standby supply current	STDBY = 1; V_{PLL2} < 1 V; 3.5 V < V_{CC} < 16 V	–	9	–	mA
PSRR	power supply rejection ratio of internal supply voltage	f = 1 kHz	50	–	–	dB
$V_{CC(blank)}$	supply voltage level for activation of continuous blanking	V_{CC} decreasing from 12 V	8.2	8.6	9.0	V
$V_{CC(blank)(min)}$	minimum supply voltage level for function of continuous blanking	V_{CC} decreasing from 12 V	2.5	3.5	4.0	V
$V_{on(VCC)}$	supply voltage level for activation of HDRV, BDRV, VOUT1, VOUT2 and HUNLOCK	V_{CC} increasing from below typical 8 V	7.9	8.3	8.7	V
$V_{off(VCC)}$	supply voltage level for deactivation of BDRV, VOUT1, VOUT2 and HUNLOCK; also sets register SOFTST	V_{CC} decreasing from above typical 8.3 V	7.7	8.1	8.5	V

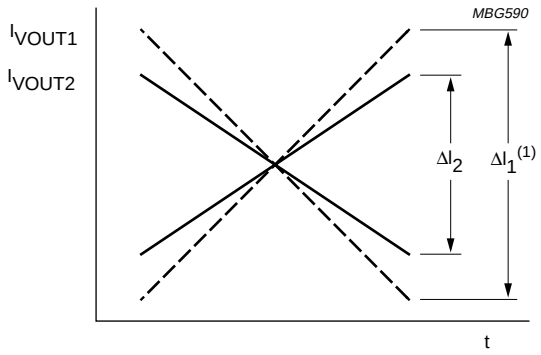
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THRESHOLDS DERIVED FROM HPLL2 VOLTAGE						
$V_{HPLL2(blank)(ul)}$	upper limit for continuous blanking		–	4.7	–	V
$V_{HPLL2(bduty)(ul)}$	upper limit for variation of BDRV duty cycle		–	3.4	–	V
$V_{HPLL2(bduty)(ll)}$	lower limit for variation of BDRV duty cycle		–	2.8	–	V
$V_{HPLL2(hduty)(ul)}$	upper limit for variation of HDRV duty cycle		–	2.8	–	V
$V_{HPLL2(hduty)(ll)}$	lower limit for variation of HDRV duty cycle		–	1.7	–	V
$V_{HPLL2(stby)(ll)}$	lower limit for VOUT1 and VOUT2 to be active via I²C-bus soft start		–	1.1	–	V
$V_{HPLL2(stby)(ul)}$	upper limit for standby voltage		–	1	–	V
$V_{HPLL2(stby)(ll)}$	lower limit for VOUT1 and VOUT2 to be active via external DC current		–	0	–	V

Notes

1. For duration of vertical blanking pulse see subheading “Vertical oscillator [oscillator frequency in application without adjustment of free-running frequency $f_{fr(V)}$]”.
2. Continuous blanking at CLBL (pin 16) will be activated, if one of the following conditions is true:
   a) No horizontal flyback pulses at HFLB (pin 1) within a line
   b) X-ray protection is triggered
   c) Voltage at HPLL2 (pin 30) is low during soft start
   d) Supply voltage at V_{CC} (pin 10) is low
   e) PLL1 unlocked while frequency-locked loop is in search mode.
3. Oscillator frequency is f_{min} when no sync input signal is present (continuous blanking at pins 16 and 17).
4. Loading of HPLL1 (pin 26) is not allowed.
5. Voltage at HPLL1 (pin 26) is fed to HBUF (pin 27) via a buffer. Disturbances caused by horizontal sync are removed by an internal sample-and-hold circuit.
6. All vertical and EW adjustments are specified at nominal vertical settings; unless otherwise specified, which means:
   a) VSIZE = 100% (register VSIZE = 127 and control bit VOVSCN = 0)
   b) VSMOD = 0 (no EHT compensation)
   c) VPOS centred (register VPOS = X and control bit VPC = 1)
   d) VLIN = 0 (register VLIN = X and control bit VSC = 1)
   e) VLINBAL = 0 (register VLINBAL = X and control bit VLC = 1)
   f) FHMULT = 0
   g) HPARAL = 0 (register HPARAL = X and control bit HPC = 1)
   h) HPINBAL = 0 (register HPINBAL = X and control bit HBC = 1)
   i) Vertical oscillator synchronized
   j) HSIZE = 255.

7. All vertical and EW adjustments in accordance with note 6, but VSIZE = 80% (register VSIZE = 63 and control bit VOVSCN = 0).
8. Value of resistor at VREF (pin 23) may not be changed.
9. The output signal at EWDRV (pin 11) may consist of horizontal pincushion + corner correction + DC shift + trapezium correction. If the VOVSCN control bit is set, and the VPOS adjustment is set to an extreme value, the tip of the parabola may be clipped at the upper limit of the EWDRV output voltage range. The waveform of corner correction will clip if the vertical sawtooth adjustment exceeds 110% of the nominal setting.
10. If f_H tracking is enabled, the amplitude of the complete EWDRV output signal (horizontal pincushion + corner correction + DC shift + trapezium) will be changed proportional to I_{HREF}. The EWDRV low level of 1.2 V remains fixed.
11. First pole of transconductance amplifier is 5 MHz without external capacitor (will become the second pole, if the OTA operates as an integrator).
12. Open-loop gain is $\frac{V_{BOP}}{V_{BIN}}$ at f = 0 with no resistive load and C_{BOP} = 10 nF [from BOP (pin 3) to GND].

Vertical and EW adjustments

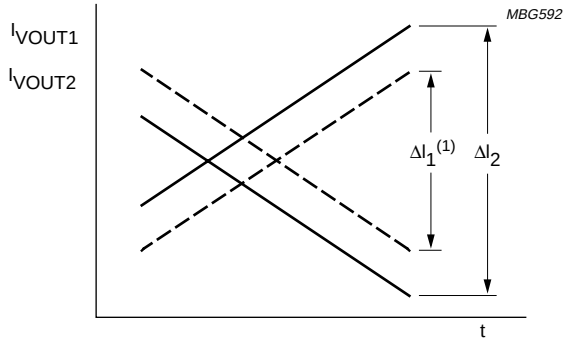


(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127, control bit VOVSCN = 0, control bit VPC = 1, control bit VSC = 1 and control bit VLC = 1.

$$VSIZE = \frac{\Delta I_2}{\Delta I_1} \times 100\%$$

$$VSMOD = \frac{\Delta I_2}{\Delta I_1} \times 100\%$$

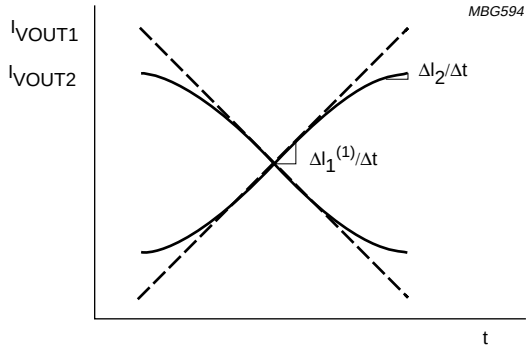
Fig.5 Adjustment of vertical size.



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127 and control bit VPC = 1.

$$VPOS = \frac{\Delta I_2 - \Delta I_1}{2 \times \Delta I_1} \times 100\%$$

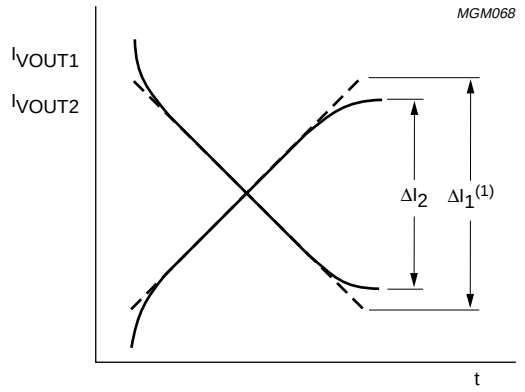
Fig.6 Adjustment of vertical position.



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127 and VLIN = 0%.

$$VLIN = \frac{\Delta I_1 - \Delta I_2}{\Delta I_1} \times 100\%$$

Fig.7 Adjustment of vertical linearity (vertical S-correction).



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127, register VOVSCN = 0, control bit VPC = 1, control bit VLIN = 1 and control bit VLINBAL = 0.

$$VLINBAL = \frac{\Delta I_1 - \Delta I_2}{2 \times \Delta I_1} \times 100\%$$

Fig.8 Adjustment of vertical linearity balance.

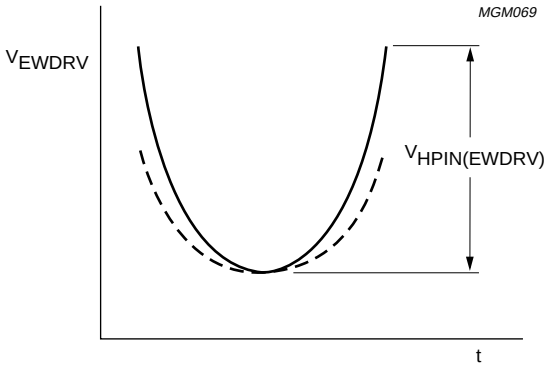


Fig.9 Adjustment of parabola amplitude at pin EWDRV.

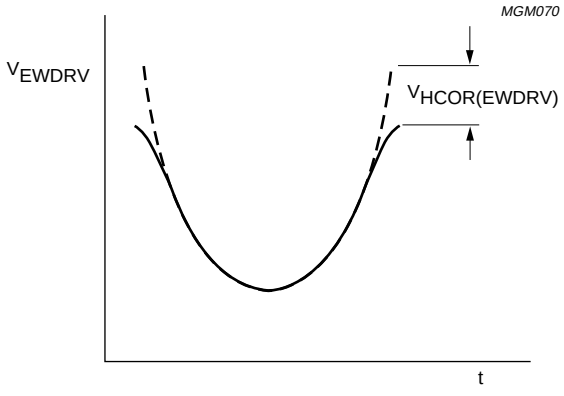


Fig.10 Influence of corner correction at pin EWDRV.

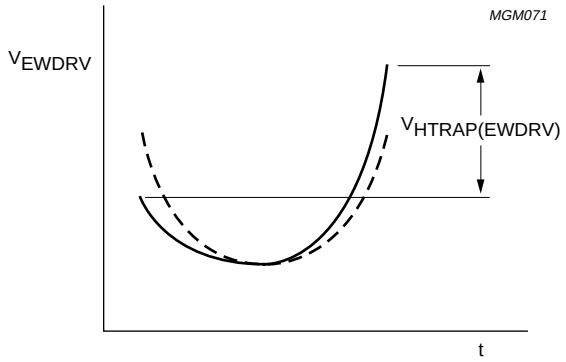


Fig.11 Influence of trapezium at pin EWDRV.

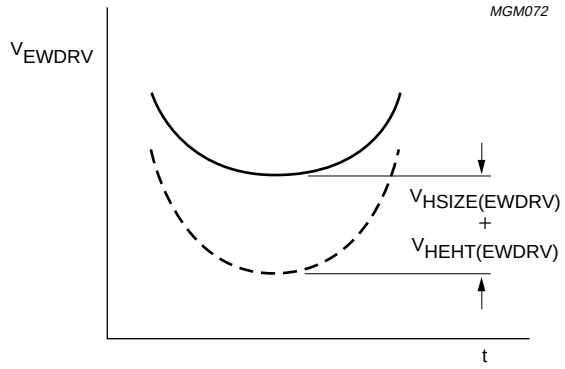


Fig.12 Influence of HSIZE and EHT compensation at pin EWDRV.

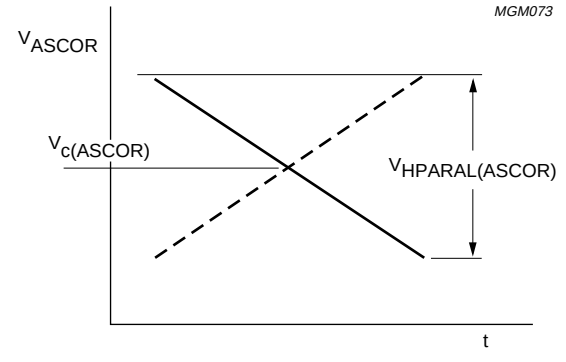


Fig.13 Adjustment of parallelogram at pin ASCOR.

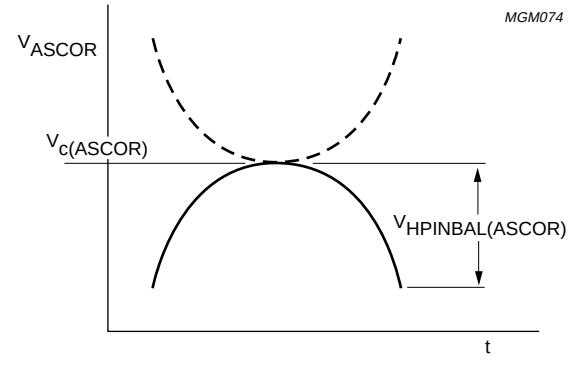


Fig.14 Adjustment of pin balance at pin ASCOR.

Pulse diagrams

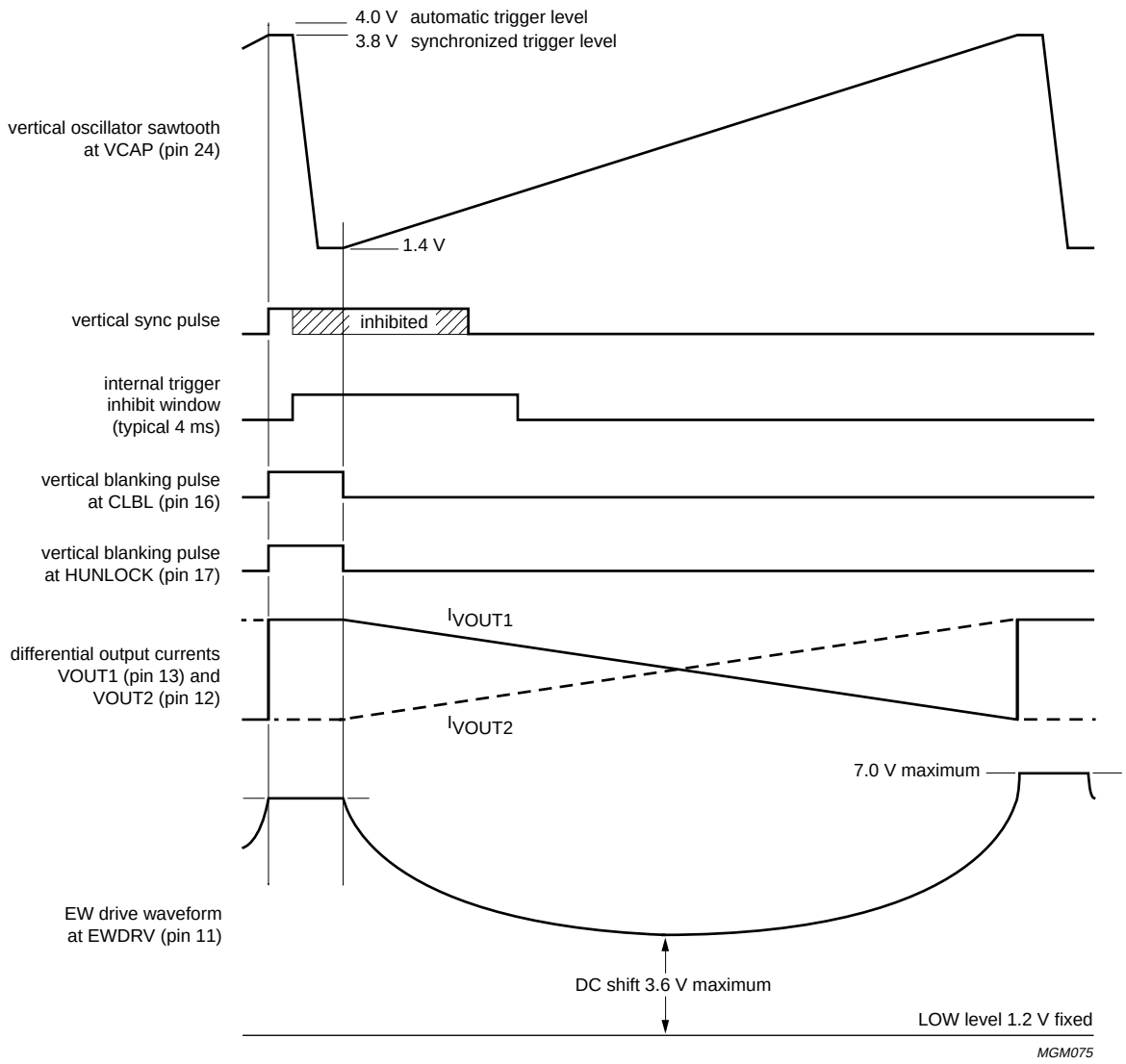


Fig.15 Pulse diagram for vertical part.

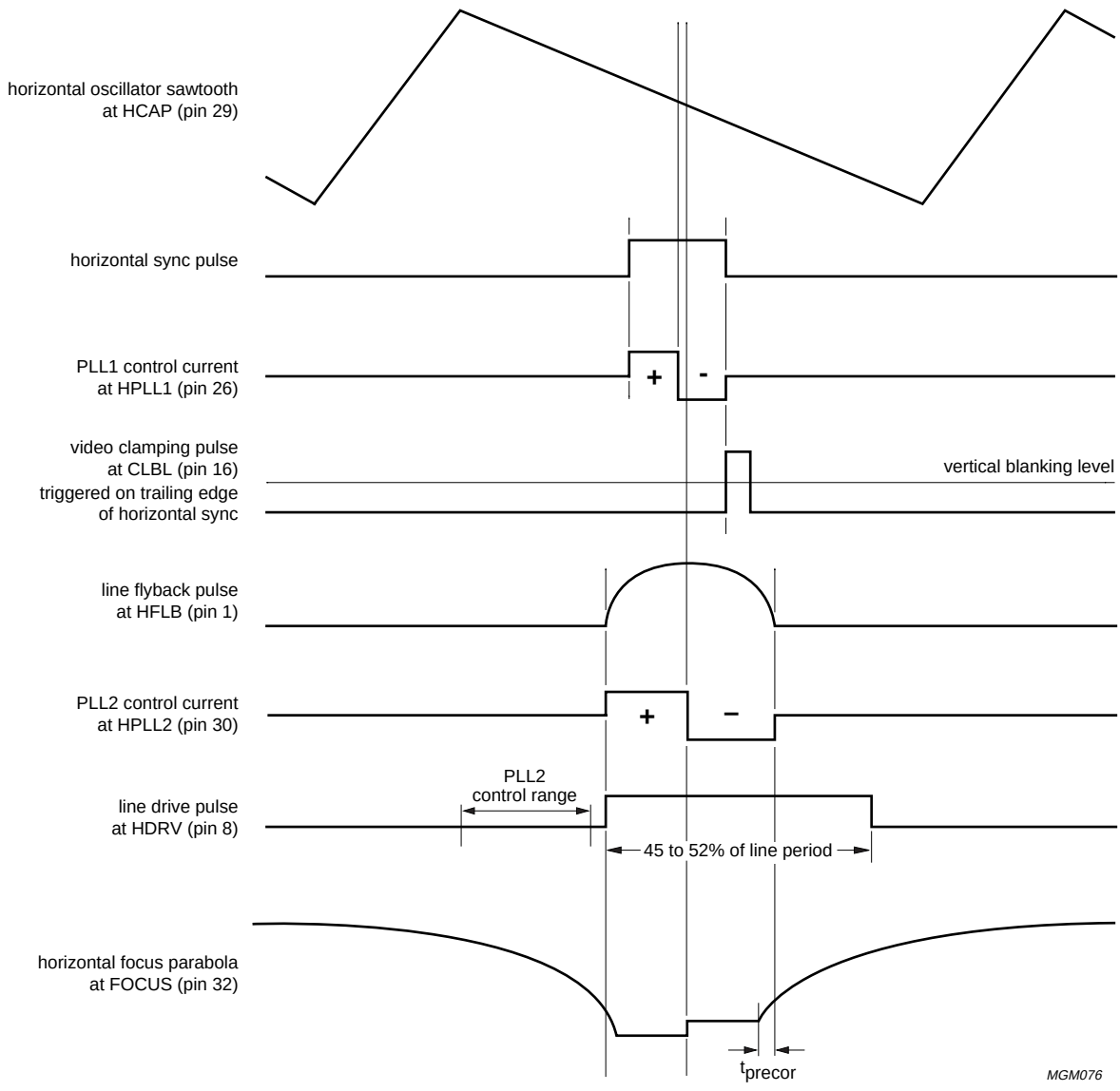


Fig.16 Pulse diagram for horizontal part.

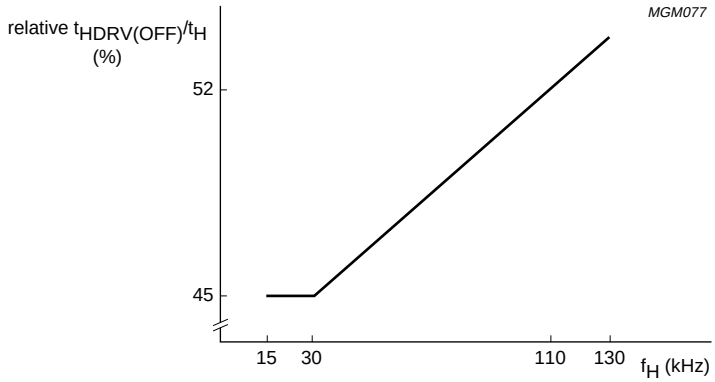
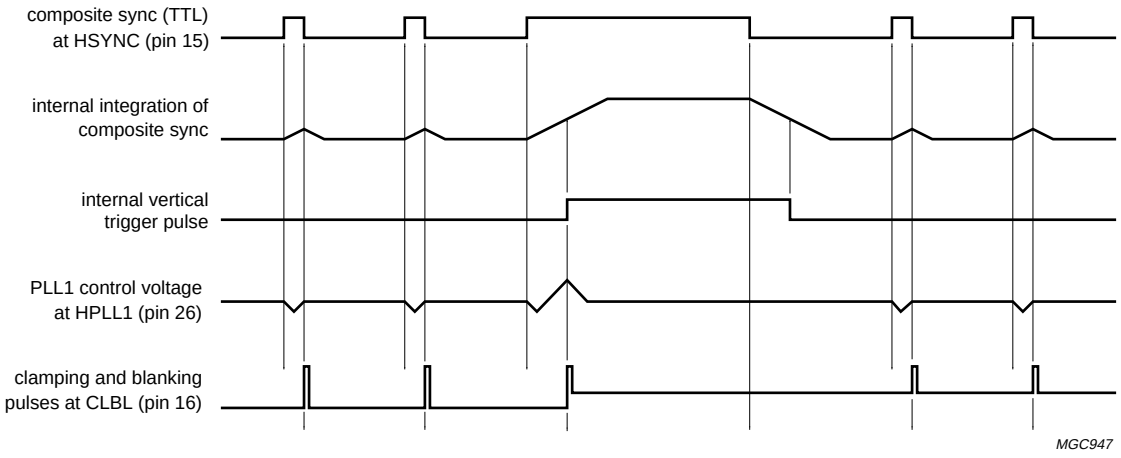
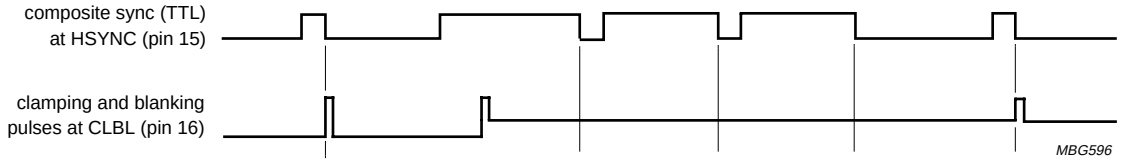


Fig.17 Relative t_{OFF} time of HDRV as a function of horizontal frequency.



a. Reduced influence of vertical sync on horizontal phase.



b. Generation of video clamping pulses during vertical sync with serration pulses.

Fig.18 Pulse diagrams for composite sync applications.

I²C-BUS PROTOCOL

I²C-bus data format

S(1)	SLAVE ADDRESS(2)	A(3)	SUBADDRESS(4)	A(3)	DATA(5)	A(3)	P(6)

Notes

1. S = START condition.
2. SLAVE ADDRESS (MAD) = 1000 1100.
3. A = acknowledge, generated by the slave. No acknowledge, if the supply voltage is below 8.3 V for start-up and 8.1 V for shut-down procedure.
4. SUBADDRESS (SAD).
5. DATA, if more than 1 byte of DATA is transmitted, then **no** auto-increment of the significant subaddress is performed.
6. P = STOP condition.

It should be noted that clock pulses according to the 400 kHz specification are accepted for 3.3 and 5 V applications (reference level = 1.8 V). Default register values after power-up are random. All registers have to be preset via software before the soft start is enabled.

Important: If the register contents are changed during the vertical scan, this might result in a visible interference on the screen. The cause for this interference is the abrupt change in picture geometry which takes effect at random locations within the visible picture.

To avoid this kind of interference, the adjustment of the critical geometry parameters HSIZE, HPOS, VSIZE and VPOS should be synchronized with the vertical flyback. This should be done in such a way that the adjustment change takes effect during the vertical blanking time (see Fig.19).

For very slow I²C-bus interfaces, it might be necessary to delay the transmission of the last byte (or only the last bit) of an I²C-bus message until the start of the vertical sync or vertical blanking.

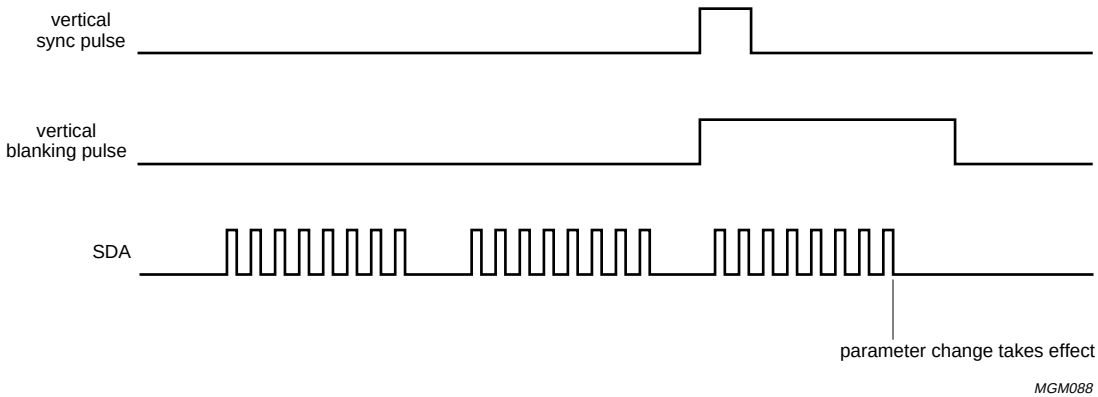


Fig.19 Timing of the I²C-bus transmission for interference-free adjustment.

Table 4 List of I²C-bus controlled switches; notes 1 and 2

BIT	FUNCTION	SAD (HEX)	REGISTER ASSIGNMENT							
			D7	D6	D5	D4	D3	D2	D1	D0
BLKDIS	0: vertical, protection and horizontal unlock blanking available at CLBL and HUNLOCK (pins 16 and 17)	01	X	#	#	#	#	#	#	D0
	1: only vertical and protection blanking available at CLBL and HUNLOCK									
HBC	0: HPINBAL (parabola) waveform enabled	01	X	#	#	#	#	#	D1	#
	1: HPINBAL (parabola) waveform disabled									
HPC	0: HPARAL (sawtooth) waveform enabled	01	X	#	#	#	#	D2	#	#
	1: HPARAL (sawtooth) waveform disabled									
AGCDIS	0: AGC in vertical oscillator active	01	X	#	#	#	D3	#	#	#
	1: AGC in vertical oscillator inhibited									
VSC	0: VLIN and HCOR adjustments enabled	01	X	#	#	D4	#	#	#	#
	1: VLIN and HCOR adjustments forced to centre value									
MOD	0: horizontal and vertical moire cancellation enabled	01	X	#	D5	#	#	#	#	#
	1: horizontal and vertical moire cancellation disabled									
TVMOD	0: TV mode at f_{min} not activated	01	X	D6	#	#	#	#	#	#
	1: TV mode at f_{min} activated									
FHMULT	0: EW output independent of horizontal frequency	0B	#	#	#	#	#	#	X	D0
	1: EW output tracks with horizontal frequency									
VOVSCN	0: vertical size 100%	0B	#	#	#	#	#	D2	X	#
	1: vertical size 116.8% for VGA350									
CLAMP	0: trailing edge for horizontal clamp	0B	#	#	#	#	D3	#	X	#
	1: leading edge for horizontal clamp									
VBLK	0: vertical blanking = 260 µs	0B	#	#	#	D4	#	#	X	#
	1: vertical blanking = 340 µs									
VLC	0: VLINBAL adjustment enabled	0B	#	#	D5	#	#	#	X	#
	1: VLINBAL adjustment forced to centre value									
VPC	0: VPOS and HTRAP adjustments enabled	0B	#	D6	#	#	#	#	X	#
	1: VPOS and HTRAP adjustments forced to centre value									
ACD	0: ASCOR disconnected from PLL2	0B	D7	#	#	#	#	#	X	#
	1: ASCOR internally connected with PLL2									
STDBY(3)	0: internal power supply enabled	0D	X	X	X	X	X	X	#	D0
	1: internal power supply disabled									
SOFTST(3)	0: soft start not released (HPLL2 (pin 30) pulled to ground)	0D	X	X	X	X	X	X	D1	#
	1: soft start is released (via HPLL2 (pin 30), power-up)									

Notes

1. X = don't care.
2. # = this bit is occupied by another function. If the register is addressed, the bit values for both functions must be transferred.
3. STDBY and SOFTST bits can be reset by internal protection circuit.

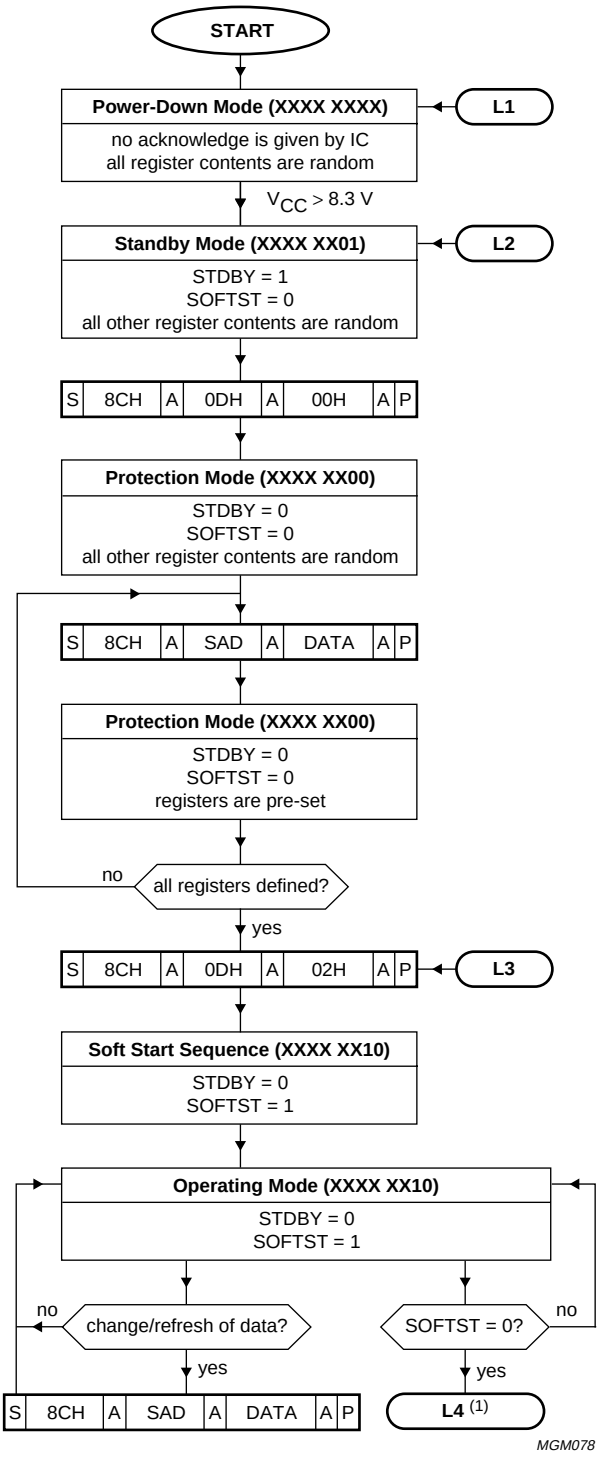
Table 5 List of I²C-bus controlled functions and those accessible by pins; notes 1 and 2

FUNCTION	NAME OF REGISTER	NUMBER OF BITS	SAD (HEX)	REGISTER ASSIGNMENT								CNTRL BIT	RANGE	FUNCTION TRACKS WITH
				D7	D6	D5	D4	D3	D2	D1	D0			
Horizontal size	HSIZE	8	00	D7	D6	D5	D4	D3	D2	D1	D0	–	0.1 to 3.6 V	HSMOD
Vertical position	VPOS	7	02	D7	D6	D5	D4	D3	D2	D1	X	VPC	±11.5%	VSMOD
Vertical linearity balance	VLINBAL	4	03	X	D6	D5	D4	D3	#	#	#	VLC	±2.5% of 100% vertical size	VSIZE, VOVSCN, VPOS and VSMOD
Moire cancellation via vertical position	VMOIRE	3	03	#	#	#	#	#	D2	D1	D0	MOD	0 to 0.08% of vertical amplitude	–
Horizontal pincushion	HPIN	6	04	X	X	D5	D4	D3	D2	D1	D0	–	0 to 1.44 V	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Moire cancellation via horizontal position	HMOIRE	5	05	X	X	X	D4	D3	D2	D1	D0	MOD	0 to 0.05% of horizontal period	–
Horizontal position	HPOS	8	06	D7	D6	D5	D4	D3	D2	D1	D0	–	±13% of horizontal period	–
Vertical linearity	VLIN	4	07	D7	D6	D5	D4	#	#	#	#	VSC	–2 to –46%	VSIZE, VOVSCN, VPOS and VSMOD
EW pin balance	HPINBAL	4	07	#	#	#	#	D3	D2	D1	D0	HBC and ACD	±1% of horizontal period	VSIZE, VOVSCN and VPOS
Vertical size	VSIZE	7	08	D7	D6	D5	D4	D3	D2	D1	X	–	60 to 100%	VSMOD
Horizontal corner correction	HCOR	5	09	X	X	X	D4	D3	D2	D1	D0	VSC	+6 to –46% of parabola amplitude	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Horizontal trapezium correction	HTRAP	4	0C	D7	D6	D5	D4	#	#	#	#	VPC	±0.33 V	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Horizontal parallelogram	HPARAL	4	0C	#	#	#	#	D3	D2	D1	D0	HPC and ACD	±1% of horizontal period	VSIZE, VOVSCN and VPOS

FUNCTION	NAME OF REGISTER	NUMBER OF BITS	SAD (HEX)	REGISTER ASSIGNMENT								CNTRL BIT	RANGE	FUNCTION TRACKS WITH
				D7	D6	D5	D4	D3	D2	D1	D0			
TDA4854														
Vertical focus	VFOCUS	3	0A	D7	D6	D5	#	#	#	#	#	–	0 to 25%	VSIZE, VOVSCN and VPOS
Horizontal focus	HFOCUS	5	0A	#	#	#	D4	D3	D2	D1	D0	–	0 to 100%	–

Notes

1. X = don’t care.
2. # = this bit is occupied by another function. If the register is addressed, the bit values for both functions must be transferred.



(1) See Fig.21.

Fig.20 I²C-bus flow for start-up.

Remarks to Fig.20:

V_{CC} < 8.3 V: As long as the supply is too low for correct operation, the IC will give no acknowledge due to internal power-on reset.

Supply current is 9 mA or less.

V_{CC} > 8.3 V: The internal POR has ended and the IC is in standby mode:

- Control bits STDBY and SOFTST are reset to their start values
- All other register contents are random
- Pin HUNLOCK is HIGH.

Set control bit STDBY = 0 to enable internal power supply.

Supply current increases from 9 to 70 mA.

Below 8.6 V register SOFTST cannot be set by I²C-bus.

Output stages are disabled.

Pin HUNLOCK is HIGH.

Set all registers to defined values.

Due to hardware configuration of the IC (no auto-increment) any register setting needs a complete 3-byte I²C-bus data transfer:
Start-Chip address-SubADdress-DATA-StoP.

Before starting the soft start sequence a delay of minimum 80 ms is necessary to obtain correct function of horizontal drive!

Set control bit SOFTST = 1 to enable the soft start sequence:

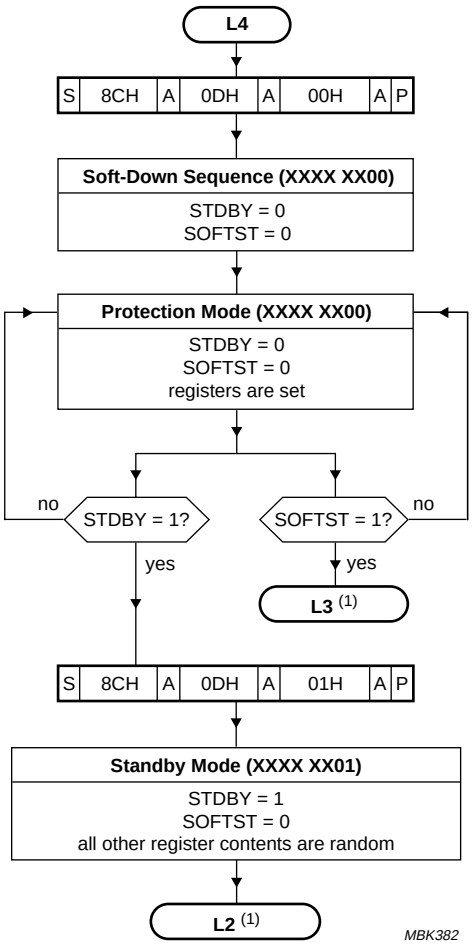
- HDRV duty cycle increases
- BDRV duty cycle increases
- VOUT1 and VOUT2 are enabled
- PLL1 and PLL2 are enabled.

IC is in full operation**.** Pin HUNLOCK is LOW if PLL1 is locked.

Any change of register content will result in immediate change of output behaviour!

Changing the control bit SOFTST to logic 0 is the only way (except power-down via pin V_{CC}) to leave the operating mode.

For starting the soft-down sequence see **L4** of Fig.21.



(1) See Fig.20.

Fig.21 I²C-bus flow for standby mode and protection mode.

Remarks to Fig.21:
Set control bit SOFTST = 0 to start the soft-down sequence:

BDRV duty cycle decreases

HDRV duty cycle decreases.

Protection mode:

Pins HDRV and BDRV are floating

Pins VOUT1 and VOUT2 are floating

Continuous blanking at pin CLBL is active

Pin HUNLOCK is floating

PLL1 and PLL2 are disabled

Register contents are kept in internal memory.

Protection mode can be left by 3 ways:

1. Entering standby mode by setting of control bits SOFTST = 0 and STDBY = 1
2. Starting soft start sequence by setting of control bit SOFTST = 1 (STDBY = don't care)
3. Supply voltage below 8.1 V.

Set control bit STDBY = 1 to enter the standby mode.
Standby Mode:

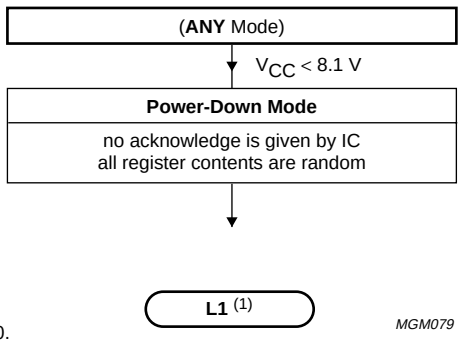
Driver outputs are floating (same as protection mode)

Supply current is 9 mA

Only I²C-bus section and protection circuits are operative

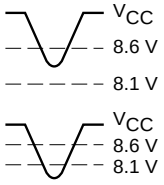
Contents of all registers except STDBY and SOFTST are lost.

See **L2** of Fig.20 for continuation.



(1) See Fig.20.

V_{CC} shut-down:
V_{CC} < 8.1 V will immediately disable all driver outputs! This function is independent from the operating mode, so it works under any condition!
Power dip:

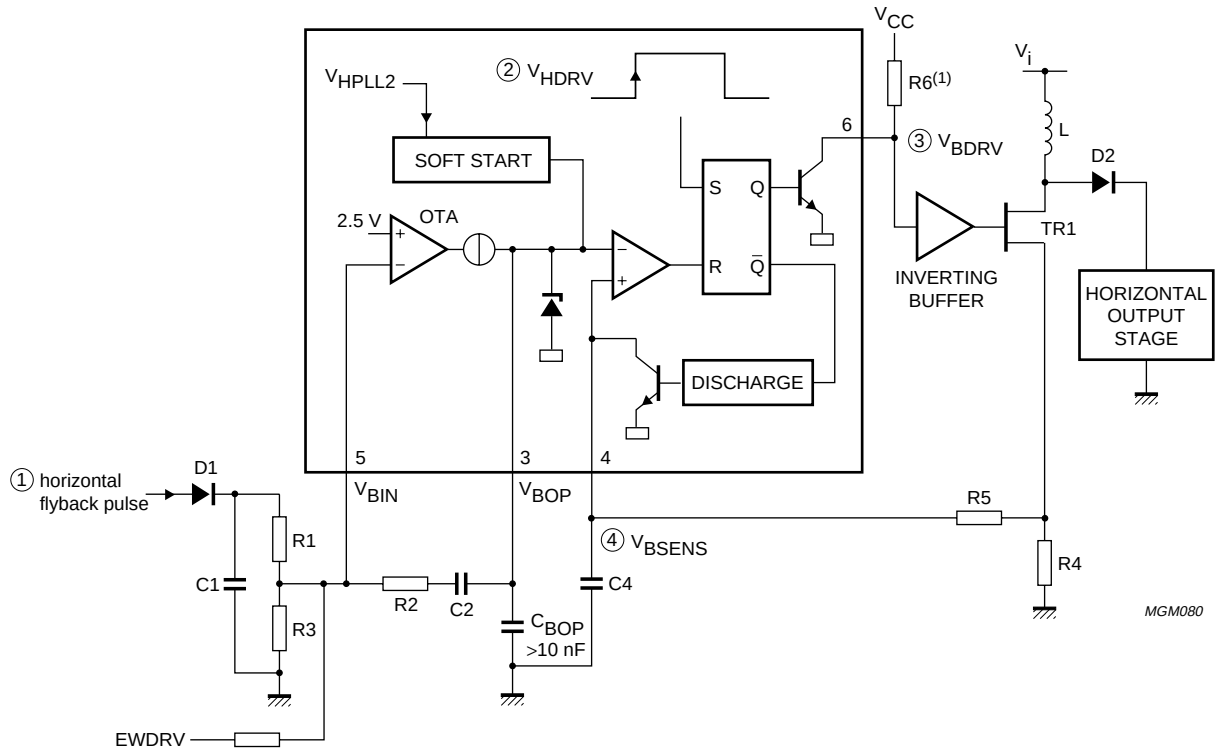


a soft-down sequency followed by a soft start sequence is generated internally.

IC enters standby mode.

Fig.22 I²C-bus flow for any mode.

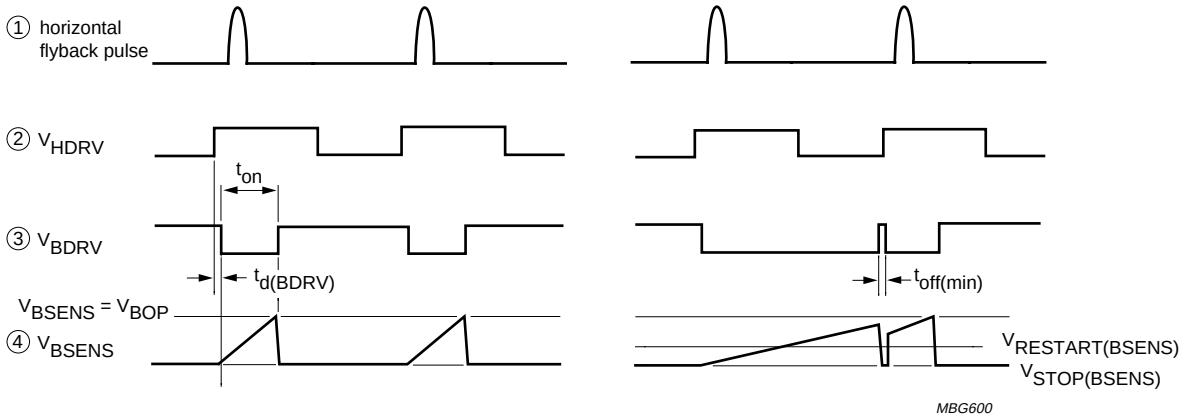
APPLICATION INFORMATION



For f < 50 kHz and C2 < 47 nF calculation formulas and behaviour of the OTA are the same as for an OP. An exception is the limited output current at BOP (pin 3). See Chapter “Characteristics”, Row Head “B+ control section (see Figs 23 and 24)”.

(1) The recommended value for R6 is 1 kΩ.

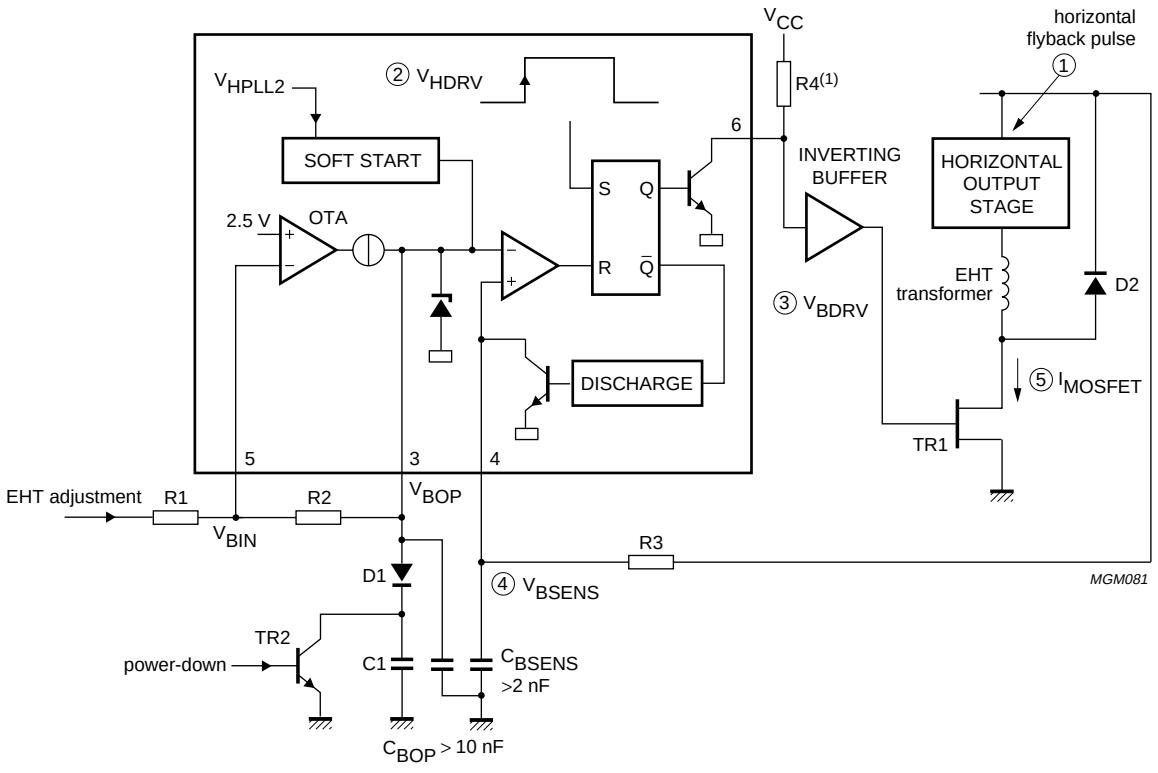
a. Feedback mode application.



b. Waveforms for normal operation.

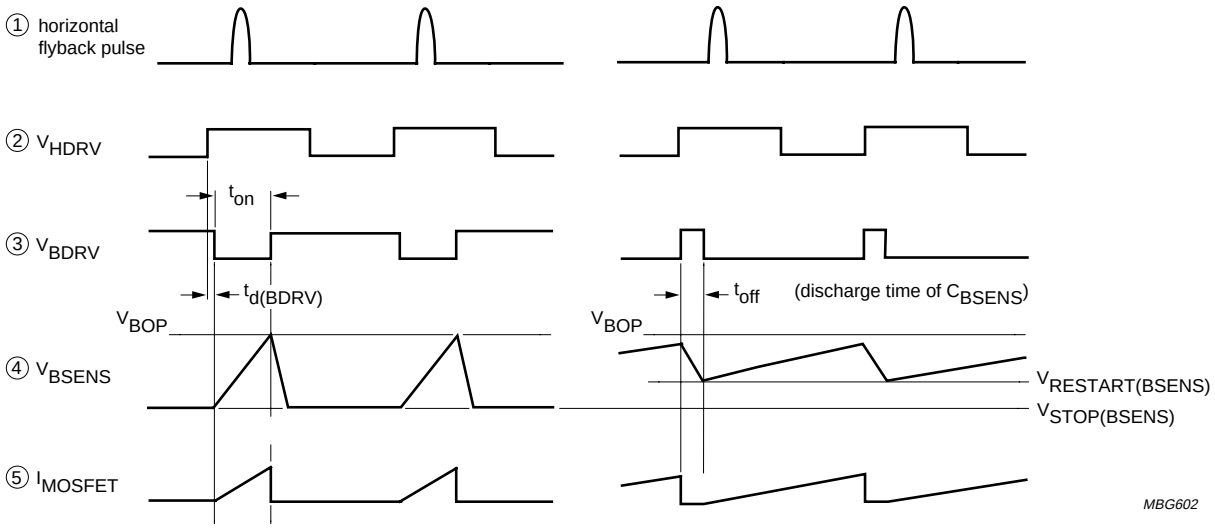
c. Waveforms for fault condition.

Fig.23 Application and timing for feedback mode.



(1) The recommended value for R4 is 1 kΩ.

a. Forward mode application.

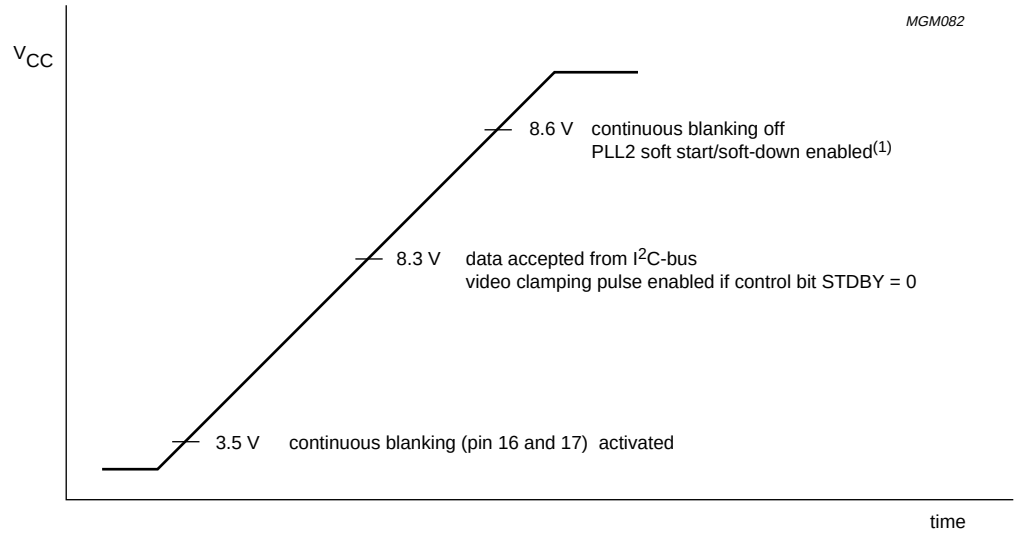


b. Waveforms for normal operation.

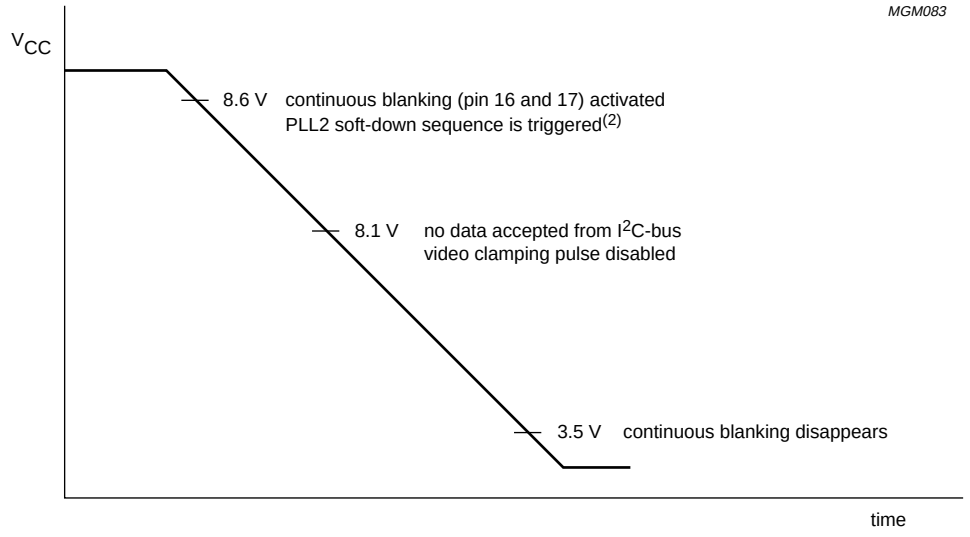
c. Waveforms for fault condition.

Fig.24 Application and timing for feed forward mode.

Start-up sequence and shut-down sequence



a. Start-up sequence.

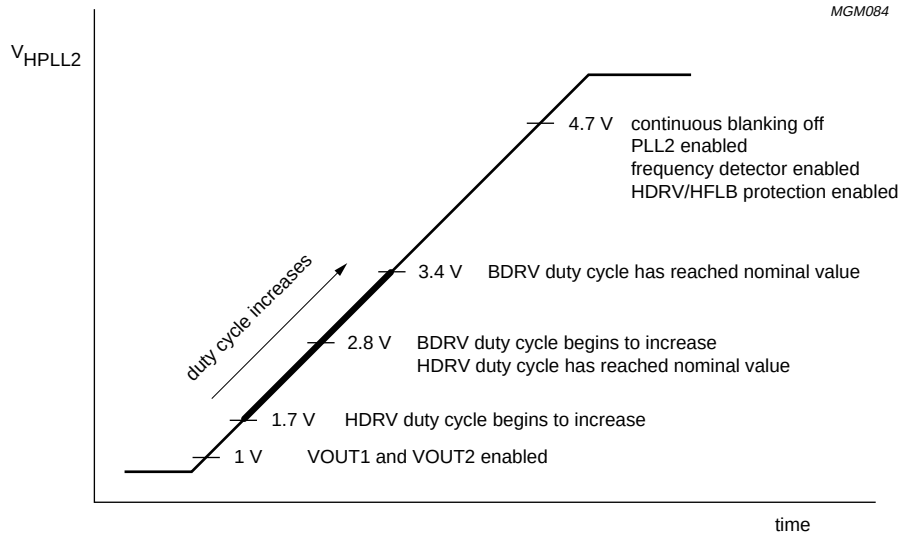


b. Shut-down sequence.

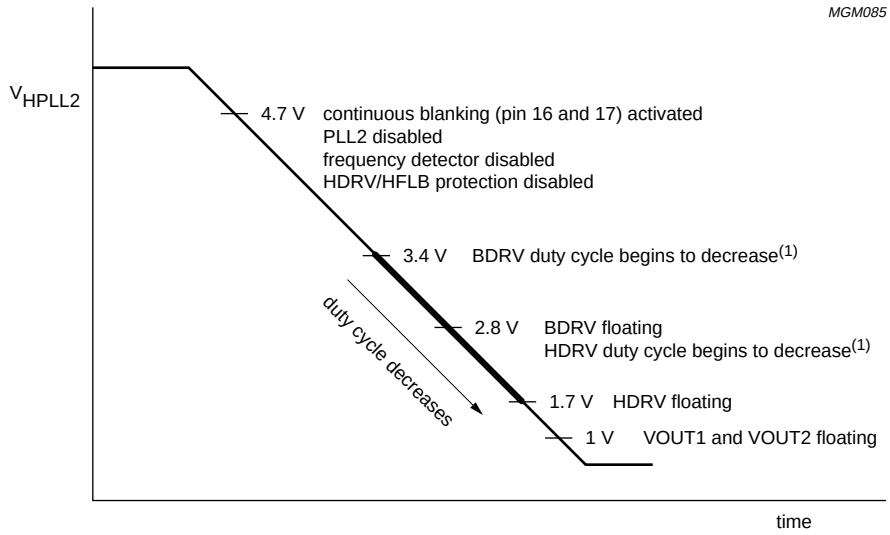
(1) See Figs 20, 21, 22, 26 and 27.
(2) See Figs 26b and 27b.

Fig.25 Start-up sequence and shut-down sequence.

PLL2 soft start sequence and PLL2 soft-down sequence



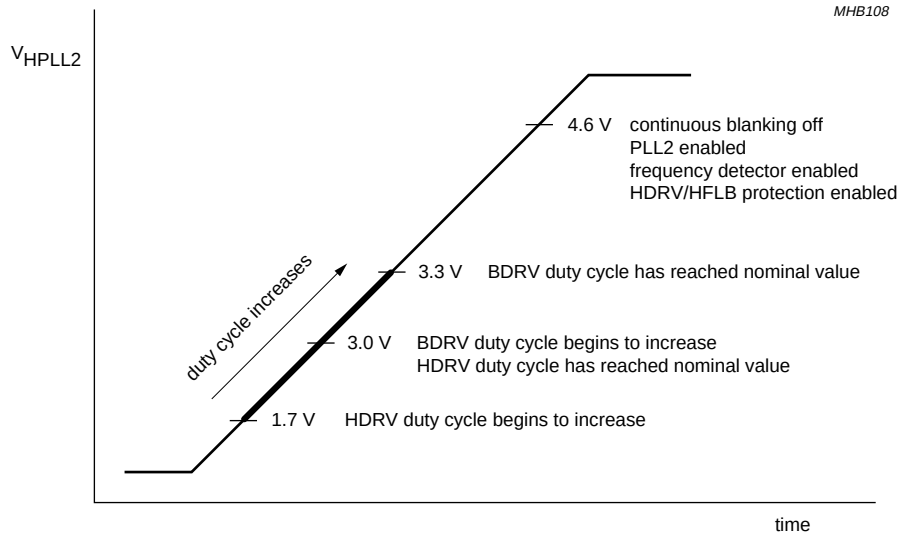
a. PLL2 soft start sequence, via the I²C-bus, if V_{CC} > 8.6 V.



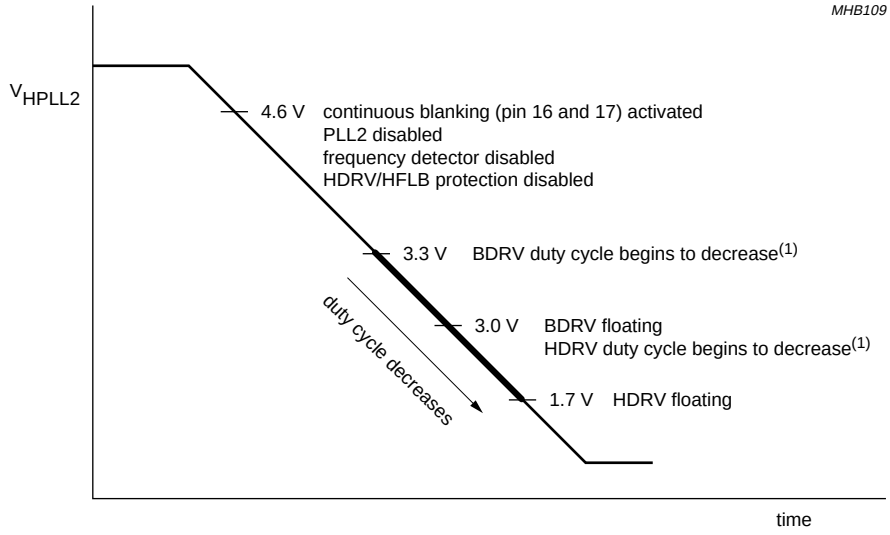
b. PLL2 soft-down sequence, via the I²C-bus, if V_{CC} > 8.6 V.

(1) HDRV, BDRV, VOUT2 and VOUT1 are floating for V_{CC} < 8.6 V.

Fig.26 PLL2 soft start sequence and PLL2 soft-down sequence via the I²C-bus.



a. PLL2 soft start sequence by external DC current, if V_{CC} > 8.6 V.



b. PLL2 soft-down sequence by external DC current, if V_{CC} > 8.6 V.

(1) HDRV, BDRV, VOUT2 and VOUT1 are floating for V_{CC} < 8.6 V.

Fig.27 PLL2 soft start sequence and PLL2 soft-down sequence by external DC current.

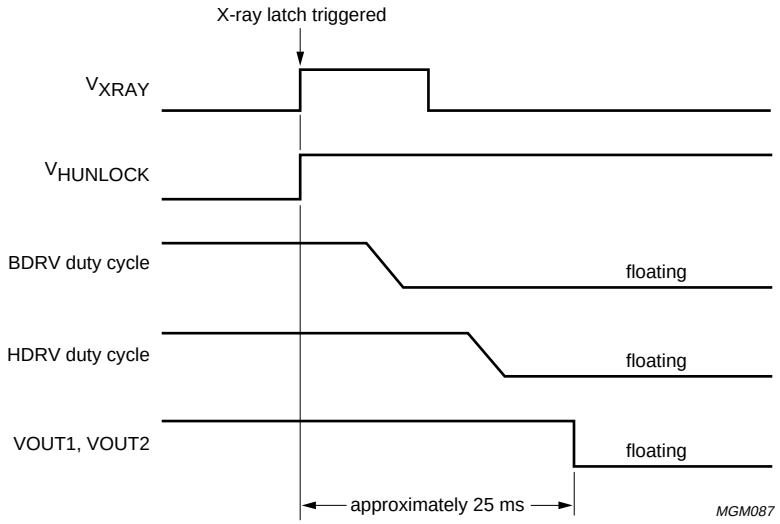
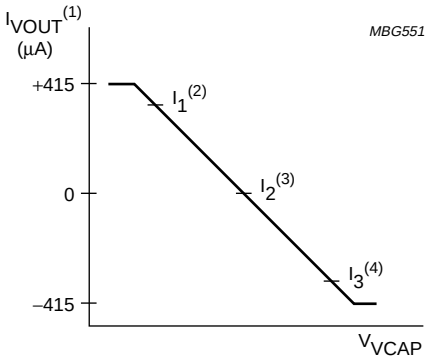


Fig.28 Activation of the soft-down sequence via pin XRAY.

Vertical linearity error



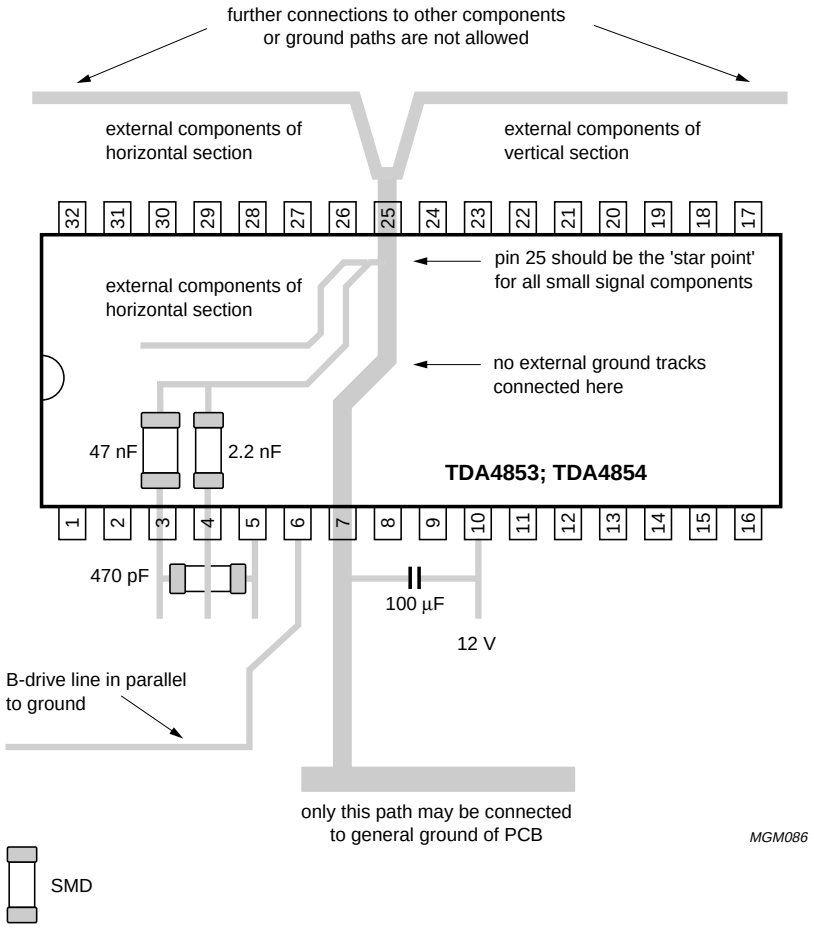
(1) $I_{VOUT} = I_{VOUT1} - I_{VOUT2}$.
(2) $I_1 = I_{VOUT}$ at $V_{VCAP} = 1.9$ V.
(3) $I_2 = I_{VOUT}$ at $V_{VCAP} = 2.6$ V.
(4) $I_3 = I_{VOUT}$ at $V_{VCAP} = 3.3$ V.

Which means: $I_0 = \frac{I_1 - I_3}{2}$

Vertical linearity error = $1 - \max\left(\frac{I_1 - I_2}{I_0} \text{ or } \frac{I_2 - I_3}{I_0}\right)$

Fig.29 Definition of vertical linearity error.

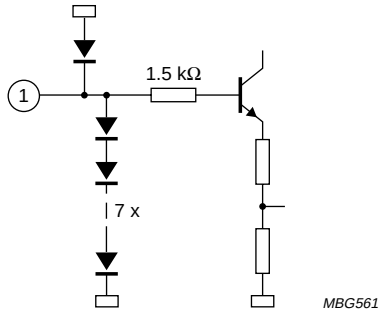
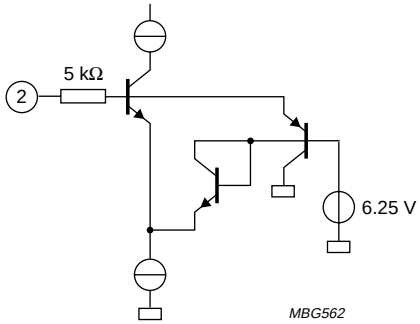
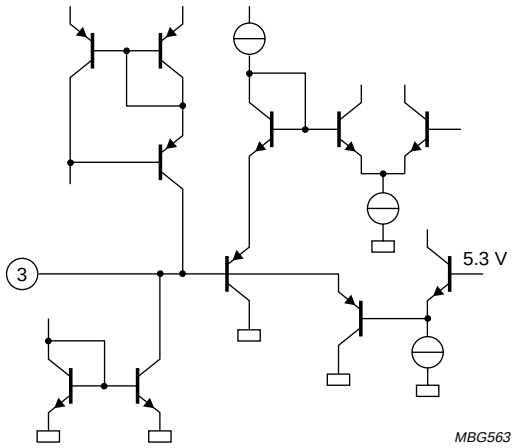
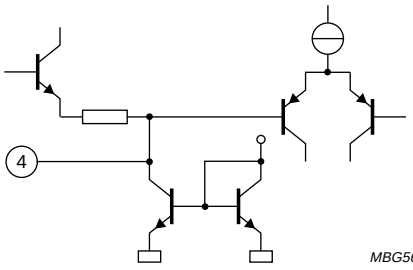
Printed-circuit board layout

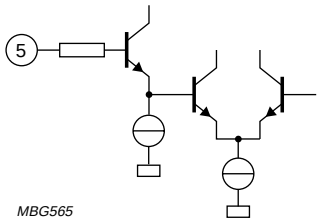
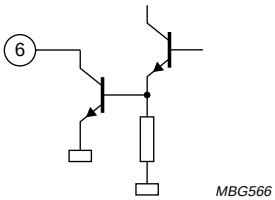
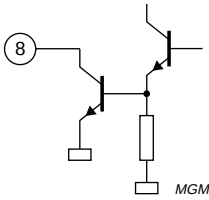
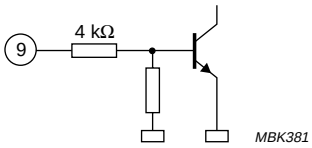
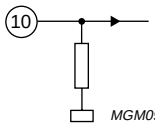
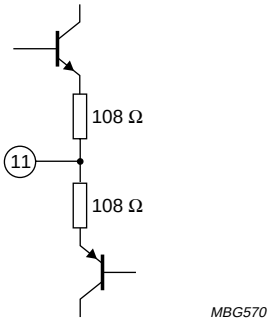


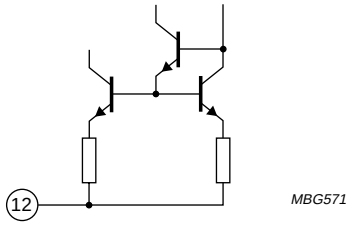
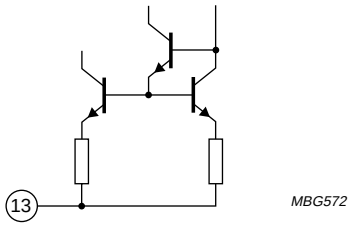
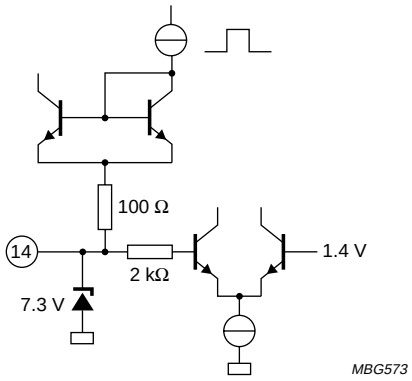
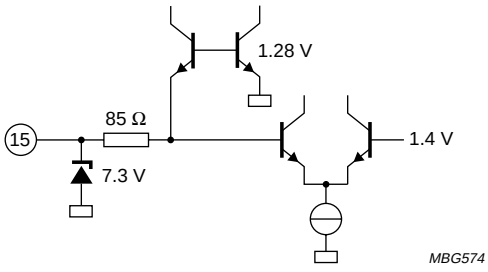
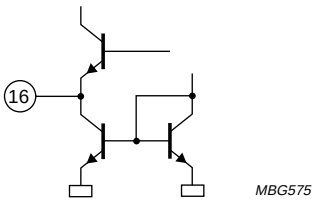
For optimum performance of the TDA4853; TDA4854 the ground paths must be routed as shown.
Only one connection to other grounds on the PCB is allowed.
Note: The tracks for HDRV and BDRV should be kept separate.

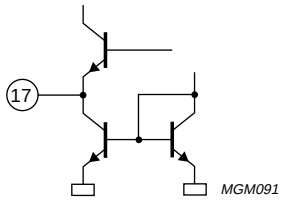
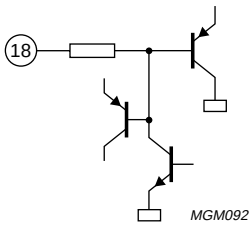
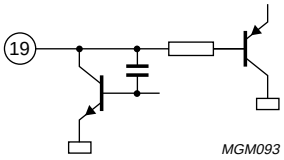
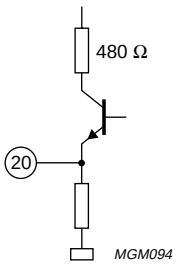
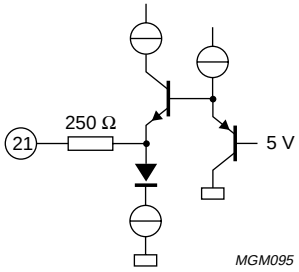
Fig.30 Hints for printed-circuit board (PCB) layout.

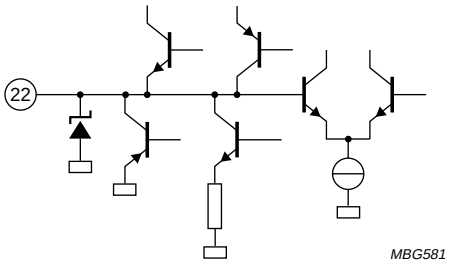
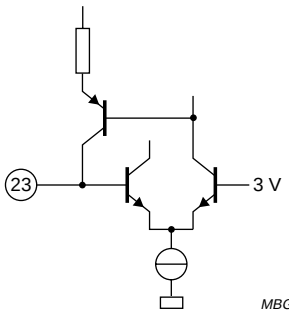
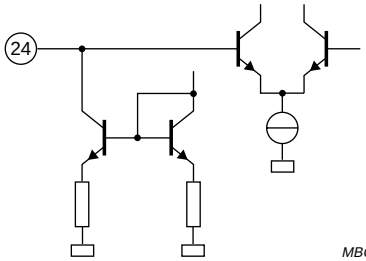
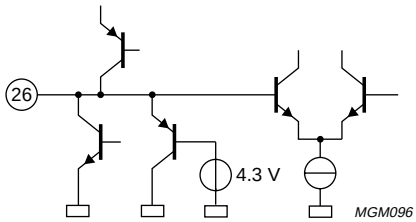
INTERNAL PIN CONFIGURATION

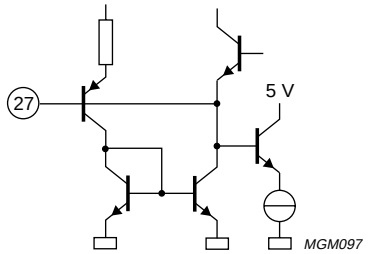
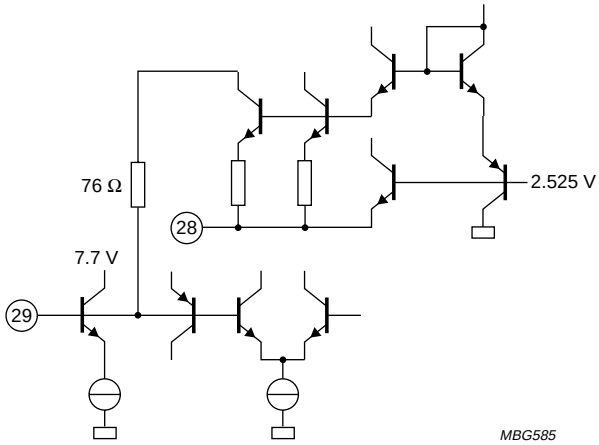
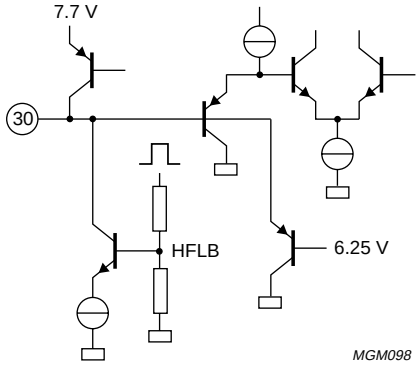
PIN	SYMBOL	INTERNAL CIRCUIT
1	HFLB	
2	XRAY	
3	BOP	
4	BSENS	

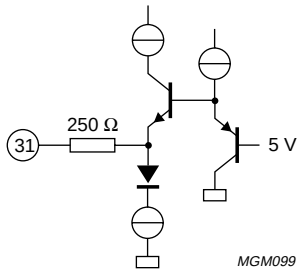
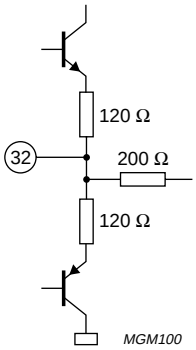
PIN	SYMBOL	INTERNAL CIRCUIT
5	BIN	
6	BDRV	
7	PGND	power ground, connected to substrate
8	HDRV	
9	XSEL	
10	V_{CC}	
11	EWDRV	

PIN	SYMBOL	INTERNAL CIRCUIT
12	VOUT2	
13	VOUT1	
14	VSYNC	
15	HSYNC	
16	CLBL	

PIN	SYMBOL	INTERNAL CIRCUIT
17	HUNLOCK	
18	SCL	
19	SDA	
20	ASCOR	
21	VSMOD	

PIN	SYMBOL	INTERNAL CIRCUIT
22	VAGC	
23	VREF	
24	VCAP	
25	SGND	signal ground
26	HPLL1	

PIN	SYMBOL	INTERNAL CIRCUIT
27	HBUF	
28	HREF	
29	HCAP	
30	HPLL2	

PIN	SYMBOL	INTERNAL CIRCUIT
31	HSMOD	
32	FOCUS(1)	

Note

1. This pin is internally connected for TDA4853.

Electrostatic discharge (ESD) protection

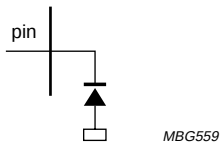


Fig.31 ESD protection for pins 4, 11 to 13, 16 and 17.

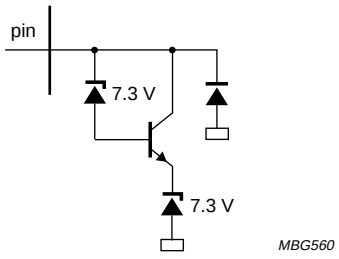
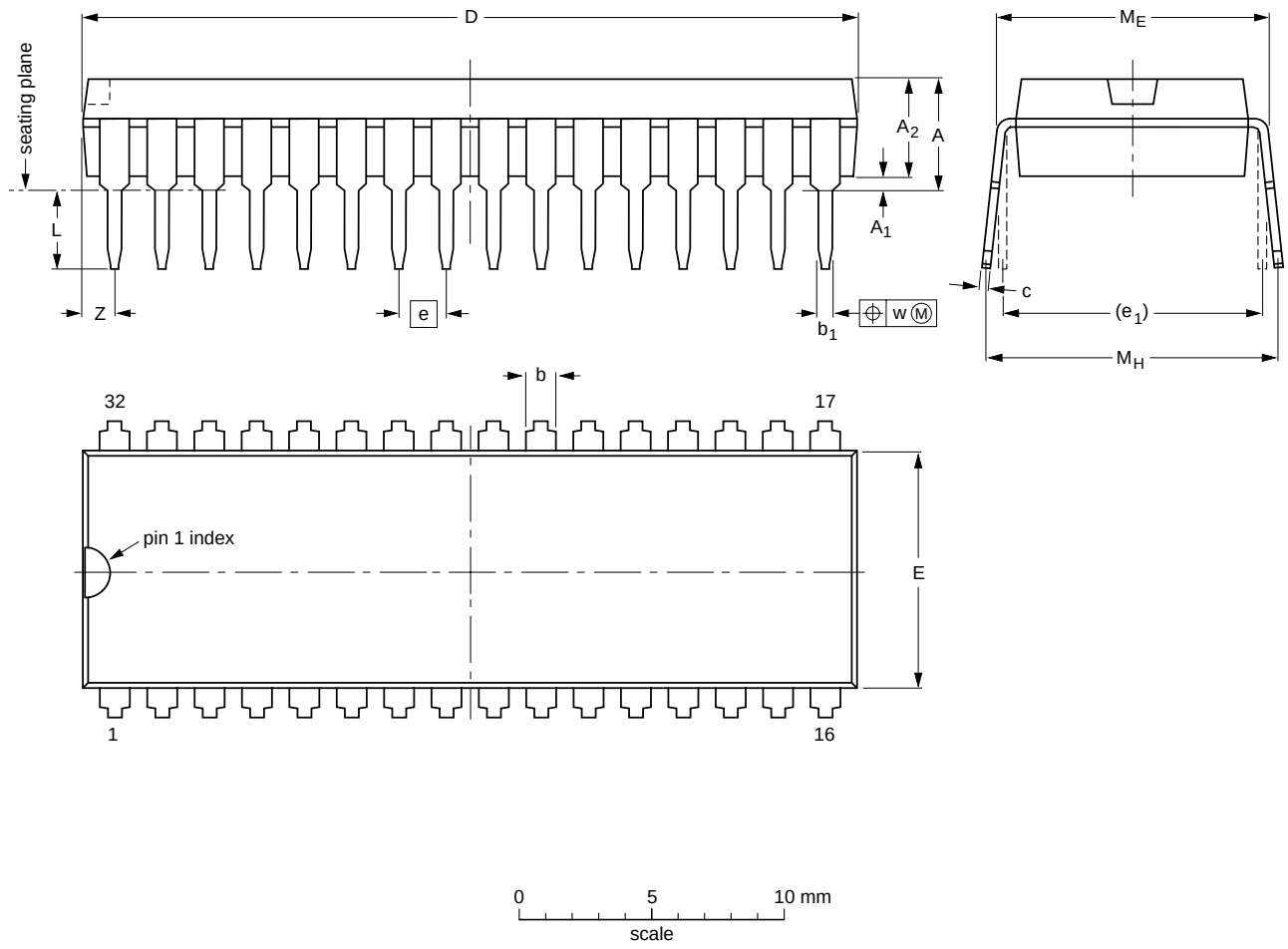


Fig.32 ESD protection for pins 2, 3, 5, 18 to 24 and 26 to 32.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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