DATA SHEET

TDA8926TH

Power stage 2 × 50 W class-D audio amplifier

Preliminary specification
Supersedes data of 2002 Feb 07

2002 Oct 22

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- High efficiency (>94%)
- Operating voltage from ±15 to ±30 V
- Very low quiescent current
- High output power
- Short-circuit proof across the load, only in combination with controller TDA8929T
- Diagnostic output
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Standby mode
- Electrostatic discharge protection (pin to pin)
- Thermally protected, only in combination with controller TDA8929T.

2 APPLICATIONS

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters).

3 GENERAL DESCRIPTION

The TDA8926TH is the switching power stage of a two-chip set for a high efficiency class-D audio power amplifier system. The system is split into two chips:

- TDA8926TH: a digital power stage in a HSOP24 power package
- TDA8929T: the analog controller chip in a SO24 package.

With this chip set a compact 2 × 50 W audio amplifier system can be built, operating with high efficiency and very low dissipation. No heatsink is required, or depending on supply voltage and load, a very small one. The system operates over a wide supply voltage range from ±15 up to ±30 V and consumes a very low quiescent current.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General; V_P = ±25 V						
V_P	supply voltage		±15	±25	±30	V
$I_{q(tot)}$	total quiescent current	no load connected	–	35	45	mA
η	efficiency	P_o = 30 W	–	94	–	%
Stereo single-ended configuration						
P_o	output power	R_L = 8 Ω; THD = 10%; V_P = ±25 V	30	37	–	W
		R_L = 4 Ω; THD = 10%; V_P = ±21 V	40	50	–	W
Mono bridge-tied load configuration						
P_o	output power	R_L = 8 Ω; THD = 10%; V_P = ±21 V	80	100	–	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8926TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

6 BLOCK DIAGRAM

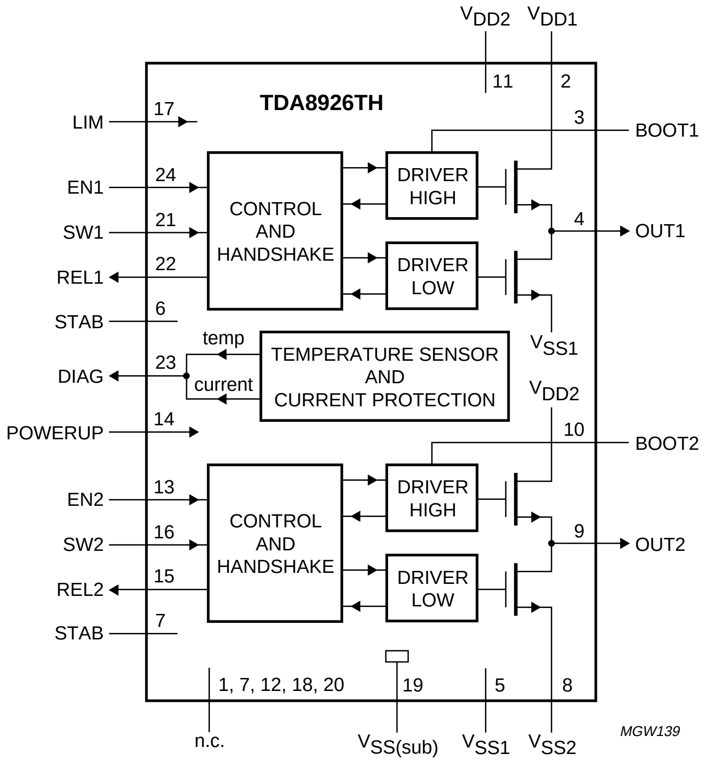


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_{DD1}	2	positive power supply; channel 1
BOOT1	3	bootstrap capacitor; channel 1
OUT1	4	PWM output; channel 1
V_{SS1}	5	negative power supply; channel 1
STAB	6	decoupling internal stabilizer for logic supply
n.c.	7	not connected
V_{SS2}	8	negative power supply; channel 2
OUT2	9	PWM output; channel 2
BOOT2	10	bootstrap capacitor; channel 2
V_{DD2}	11	positive power supply; channel 2
n.c.	12	not connected
EN2	13	digital enable input; channel 2
POWERUP	14	enable input for switching on internal reference sources
REL2	15	digital control output; channel 2
SW2	16	digital switch input; channel 2
LIM	17	pin reserved for testing; connect to V_{SS} in the application
n.c.	18	not connected
$V_{SS(sub)}$	19	negative supply (substrate)
n.c.	20	not connected
SW1	21	digital switch input; channel 1
REL1	22	digital control output; channel 1
DIAG	23	digital open-drain output for overtemperature and overcurrent report
EN1	24	digital enable input; channel 1

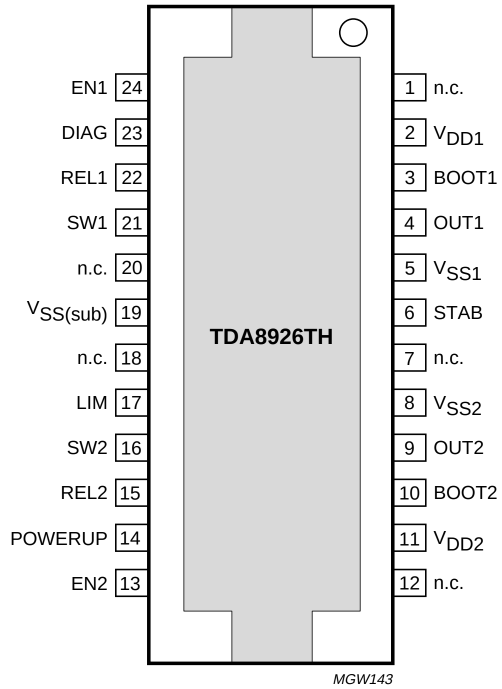


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The combination of the TDA8926TH and the controller TDA8929T produces a two-channel audio power amplifier system using the class-D technology (see Fig.3). In the TDA8929T controller the analog audio input signal is converted into a digital Pulse Width Modulation (PWM) signal.

The power stage TDA8926TH is used for driving the low-pass filter and the loudspeaker load. It performs a level shift from the low-power digital PWM signal, at logic levels, to a high-power PWM signal that switches between the main supply lines. A 2nd-order low-pass filter converts the PWM signal into an analog audio signal across the loudspeaker.

For a description of the controller, see data sheet *“TDA8929T, Controller class-D audio amplifier”*.

8.1 Power stage

The power stage contains the high-power DMOS switches, the drivers, timing and handshaking between the power switches and some control logic. For protection, a temperature sensor and a maximum current detector are built-in on the chip.

For interfacing with the controller chip the following connections are used:

- Switch (pins SW1 and SW2): digital inputs; switching from V_{SS} to V_{SS} + 12 V and driving the power DMOS switches
- Release (pins REL1 and REL2): digital outputs; switching from V_{SS} to V_{SS} + 12 V; follow SW1 and SW2 with a small delay
- Enable (pins EN1 and EN2): digital inputs; at a level of V_{SS} the power DMOS switches are open and the PWM outputs are floating; at a level of V_{SS} + 12 V the power stage is operational and controlled by the switch pin if pin POWERUP is at V_{SS} + 12 V
- Power-up (pin POWERUP): analog input; at LOW level with respect to V_{SS} the device is in standby mode and the supply current is practically zero. With a HIGH level on this pin, the device is in operating mode
- Diagnostics (pin DIAG): digital open-drain output; pulled to V_{SS} if the temperature or maximum current is exceeded.

8.2 Protection

Temperature and short-circuit protection sensors are included in the TDA8926TH. The protection circuits are operational only in combination with the controller TDA8929T. In the event that the maximum current or maximum temperature is exceeded the diagnostic output is activated. The controller has to take appropriate measures by shutting down the system.

8.2.1 OVERTEMPERATURE

If the junction temperature (T_j) exceeds 150 °C, then pin DIAG becomes LOW. The diagnostic pin is released if the temperature is dropped to approximately 130 °C, so there is a hysteresis of approximately 20 °C.

8.2.2 SHORT-CIRCUIT ACROSS THE LOUDSPEAKER TERMINALS

When the loudspeaker terminals are short-circuited This will be detected by the current protection. If the output current exceeds the maximum output current of 5 A, then pin DIAG becomes LOW. The controller should shut down the system to prevent damage. Using the TDA8929T the system is shut down within 1 µs, and after 220 ms it will attempt to restart the system again. During this time the dissipation is very low, therefore the average dissipation during a short circuit is practically zero.

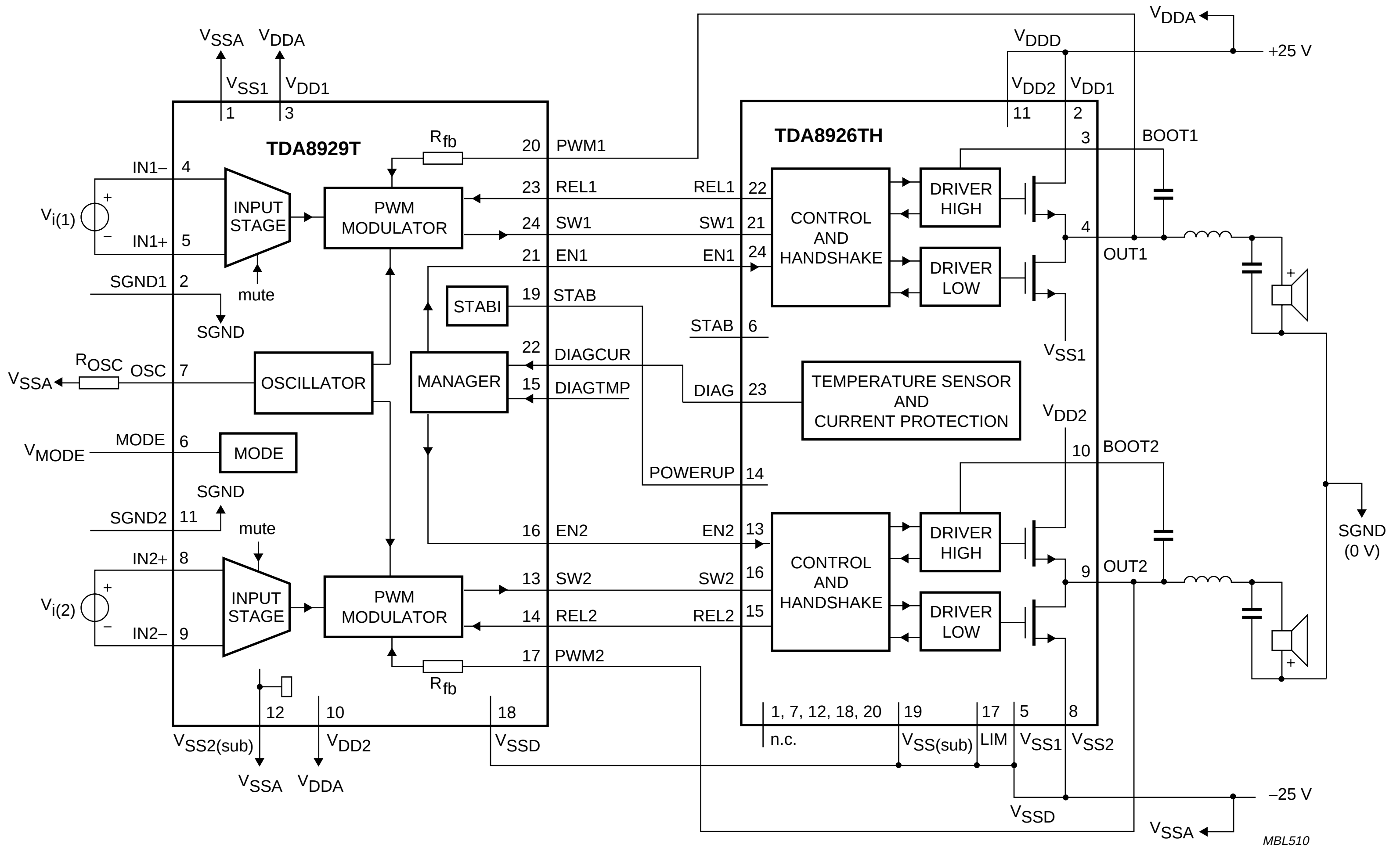


Fig.3 Typical application schematic of the class-D system using the controller TDA8929T and the TDA8926TH.

8.3 BTL operation

BTL operation can be achieved by driving the audio input channels of the controller in the opposite phase and by connecting the loudspeaker with a BTL output filter between the two outputs (pins OUT1 and OUT2) of the power stage (see Fig.4).

In this way the system operates as a mono BTL amplifier and with the same loudspeaker impedance a four times higher output power can be obtained.

For more information see Chapter 15.

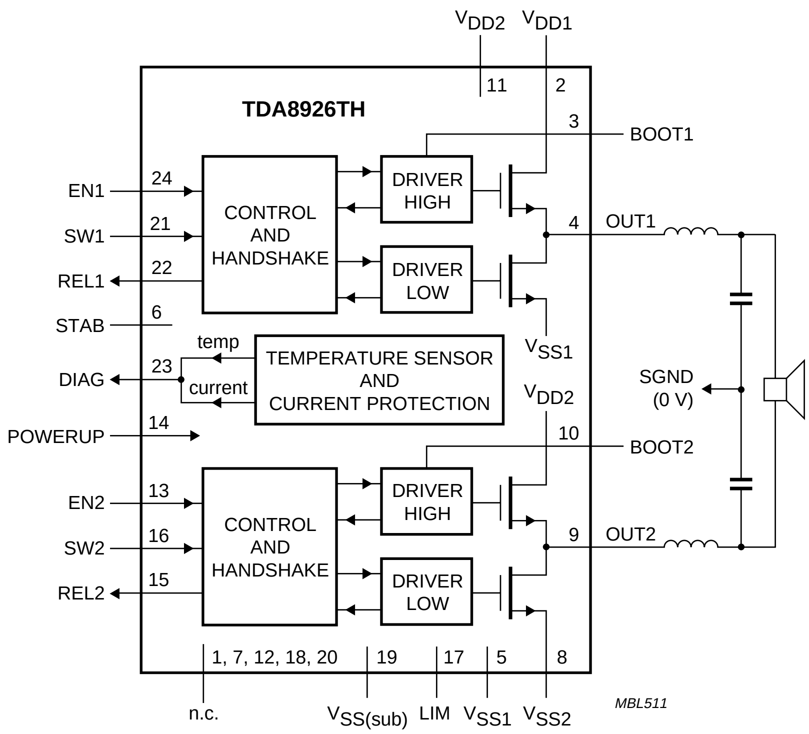


Fig.4 Mono BTL application.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rate System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	±30	V
$V_{P(sc)}$	supply voltage for short-circuits across the load		–	±30	V
I_{ORM}	repetitive peak current in output pins		–	5	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
$V_{es(HBM)}$	electrostatic discharge voltage (HBM)	note 1			
		all pins with respect to V_{DD} (class 1a)	–1000	+1000	V
		all pins with respect to V_{SS} (class 1a)	–1000	+1000	V
		all pins with respect to each other (class 1a)	–500	+500	V
$V_{es(MM)}$	electrostatic discharge voltage (MM)	note 2			
		all pins with respect to V_{DD} (class A1)	–150	+150	V
		all pins with respect to V_{SS} (class B)	–200	+200	V
		all pins with respect to each other (class A1)	–100	+100	V

Notes

1. Human Body Model (HBM); R_s = 1500 Ω; C = 100 pF.
2. Machine Model (MM); R_s = 10 Ω; C = 200 pF; L = 0.75 μH.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air	1	K/W

11 QUALITY SPECIFICATION

In accordance with *“SNW-FQ611-part D”* if this device is used as an audio amplifier (except for ESD, see also Chapter 9).

12 DC CHARACTERISTICS

V_P = ±25 V; T_{amb} = 25 °C; measured in test diagram of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	±15	±25	±30	V
I_{stb}	standby current	$V_{EN1} = V_{EN2}$ = 0 V; $V_{POWERUP}$ = 0 V	–	25	100	μA
$I_{q(tot)}$	total quiescent current	no load connected	–	35	45	mA
		outputs floating	–	5	10	mA
Internal stabilizer logic supply (pin STAB)						
$V_{O(STAB)}$	stabilizer output voltage		11	13	15	V
Switch inputs (pins SW1 and SW2)						
V_{IH}	HIGH-level input voltage	referenced to V_{SS}	10	–	V_{STAB}	V
V_{IL}	LOW-level input voltage	referenced to V_{SS}	0	–	2	V
Control outputs (pins REL1 and REL2)						
V_{OH}	HIGH-level output voltage	referenced to V_{SS}	10	–	V_{STAB}	V
V_{OL}	LOW-level output voltage	referenced to V_{SS}	0	–	2	V
Diagnostic output (pin DIAG, open-drain)						
V_{OL}	LOW-level output voltage	I_{DIAG} = 1 mA; note 2	0	–	1.0	V
I_{LO}	output leakage current	no error condition	–	–	50	μA
Enable inputs (pins EN1 and EN2)						
V_{IH}	HIGH-level input voltage	referenced to V_{SS}	–	9	V_{STAB}	V
V_{IL}	LOW-level input voltage	referenced to V_{SS}	0	5	–	V
$V_{EN(hys)}$	hysteresis voltage		–	4	–	V
$I_{I(EN)}$	input current		–	–	300	μA
Switching-on input (pin POWERUP)						
$V_{POWERUP}$	switching-on input voltage	referenced to V_{SS}				
		operating level	5	–	12	V
		standby level	0	–	2	V
$I_{I(POWERUP)}$	input current	$V_{POWERUP}$ = 12 V	–	100	170	μA
Temperature protection						
T_{diag}	temperature activating diagnostic	$V_{DIAG} = V_{DIAG(LOW)}$	150	–	–	°C
T_{hys}	hysteresis on temperature diagnostic	$V_{DIAG} = V_{DIAG(LOW)}$	–	20	–	°C

Notes

1. The circuit is DC adjusted at V_P = ±15 to ±30 V.
2. Temperature sensor or maximum current sensor activated.

13 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single-ended application; note 1						
P_o	output power	R_L = 8 Ω; THD = 0.5%; V_P = ±25 V	25[2]	30	–	W
		R_L = 8 Ω; THD = 10%; V_P = ±25 V	30[2]	37	–	W
		R_L = 4 Ω; THD = 0.5%; V_P = ±21 V	30[2]	40	–	W
		R_L = 4 Ω; THD = 10%; V_P = ±21 V	40[2]	50	–	W
THD	total harmonic distortion	P_o = 1 W; note 3				
		f_i = 1 kHz	–	0.01	0.05	%
		f_i = 10 kHz	–	0.1	–	%
$G_{v(cl)}$	closed-loop voltage gain		29	30	31	dB
η	efficiency	P_o = 30 W; f_i = 1 kHz; note 4	–	94	–	%
Mono BTL application; note 5						
P_o	output power	R_L = 8 Ω; V_P = ±21 V				
		THD = 0.5%	70[2]	80	–	W
		THD = 10%	80[2]	100	–	W
THD	total harmonic distortion	P_o = 1 W; note 3				
		f_i = 1 kHz	–	0.01	0.05	%
		f_i = 10 kHz	–	0.1	–	%
$G_{v(cl)}$	closed loop voltage gain		35	36	37	dB
η	efficiency	P_o = 30 W; f_i = 1 kHz; note 4	–	94	–	%

Notes

1. V_P = ±25 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 310 kHz; R_s = 0.1 Ω (series resistance of filter coil); T_{amb} = 25 °C; measured in reference design (SE application) shown in Fig.7; unless otherwise specified.
2. Indirectly measured; based on $R_{ds(on)}$ measurement.
3. Total Harmonic Distortion (THD) is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a low-order low-pass filter a significantly higher value will be found, due to the switching frequency outside the audio band.
4. Efficiency for power stage; output power measured across the loudspeaker load.
5. V_P = ±25 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 310 kHz; R_s = 0.1 Ω (series resistance of filter coil); T_{amb} = 25 °C; measured in reference design (BTL application) shown in Fig.4; unless otherwise specified.

14 SWITCHING CHARACTERISTICS

$V_P = \pm 25$ V; $T_{amb} = 25$ °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM outputs (pins OUT1 and OUT2); see Fig.5						
t_r	rise time		–	30	–	ns
t_f	fall time		–	30	–	ns
t_{blank}	blanking time		–	70	–	ns
t_{PD}	propagation delay	from pin SW1 (SW2) to pin OUT1 (OUT2)	–	20	–	ns
$t_{W(min)}$	minimum pulse width	note 1	–	220	270	ns
$R_{ds(on)}$	on-resistance of the output transistors		–	0.2	0.3	Ω

Note

1. When used in combination with controller TDA8929T, the effective minimum pulse width during clipping is $0.5t_{W(min)}$.

14.1 Duty factor

For the practical useable minimum and maximum duty factor (δ) which determines the maximum output power:

$$\frac{t_{W(min)} \times f_{osc}}{2} \times 100\% < \delta < \left(1 - \frac{t_{W(min)} \times f_{osc}}{2}\right) \times 100\%$$

Using the typical value this becomes 3.5% < δ < 96.5%.

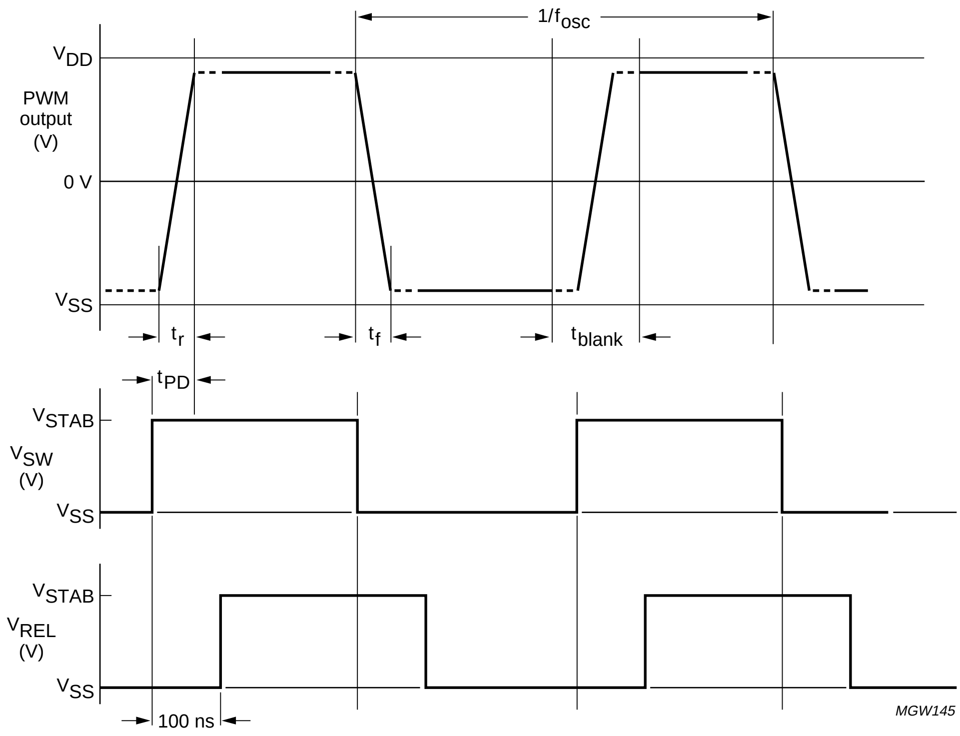


Fig.5 Timing diagram PWM output, switch and release signals.

15 TEST AND APPLICATION INFORMATION

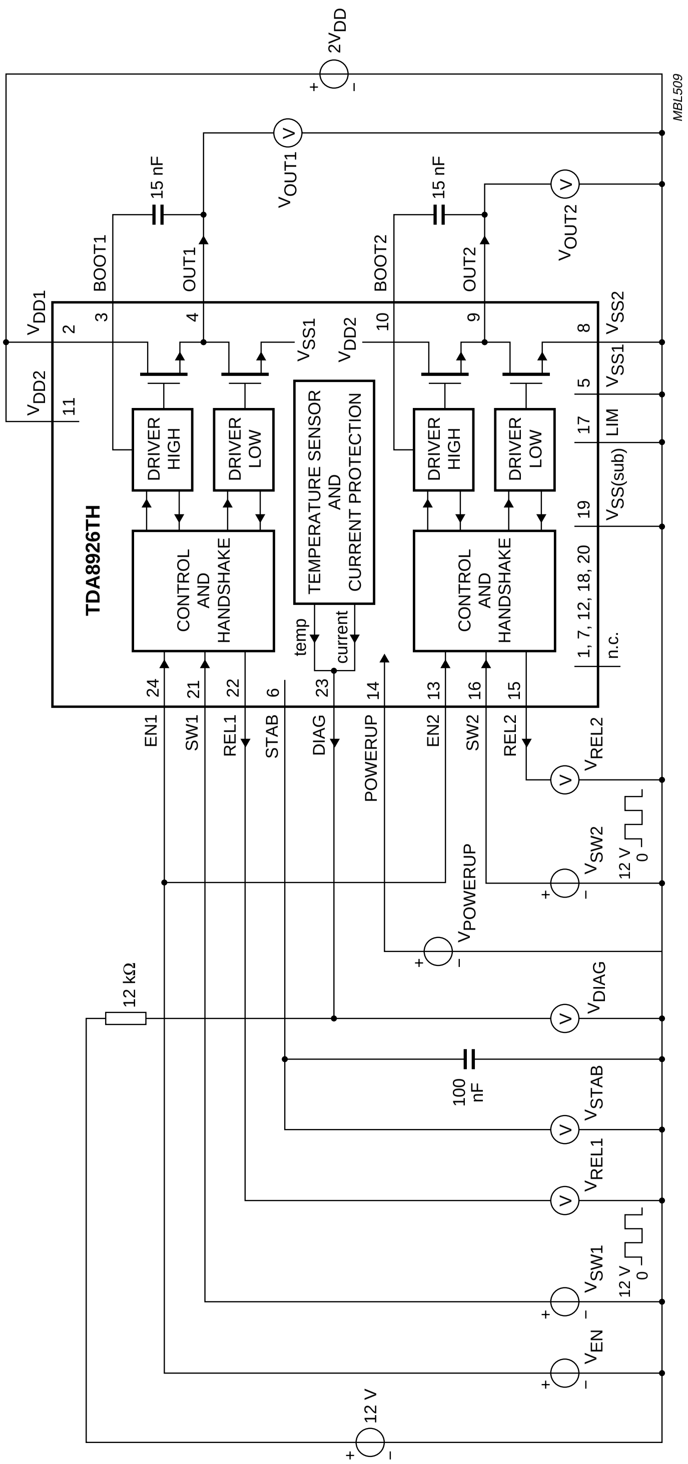


Fig.6 Test diagram.

15.1 BTL application

When using the system in a mono BTL application (for more output power), the inputs of both channels of the PWM modulator must be connected in parallel; the phase of one of the inputs must be inverted. In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

15.2 Package ground connection

The heatsink of the TDA8926TH is connected internally to V_{SS}.

15.3 Output power

The output power in single-ended applications can be estimated using the formula

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{(R_L + R_{ds(on)} + R_s)} \times V_P \times (1 - t_{W(min)} \times f_{osc})\right]^2}{2 \times R_L}$$

The maximum current $I_{O(max)} = \frac{[V_P \times (1 - t_{W(min)} \times f_{osc})]}{R_L + R_{ds(on)} + R_s}$ should not exceed 5 A.

The output power in BTL applications can be estimated using the formula

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{R_L + 2 \times (R_{ds(on)} + R_s)} \times 2V_P \times (1 - t_{W(min)} \times f_{osc})\right]^2}{2 \times R_L}$$

The maximum current $I_{O(max)} = \frac{[2V_P \times (1 - t_{W(min)} \times f_{osc})]}{R_L + 2 \times (R_{ds(on)} + R_s)}$ should not exceed 5 A.

Where:

R_L = load impedance

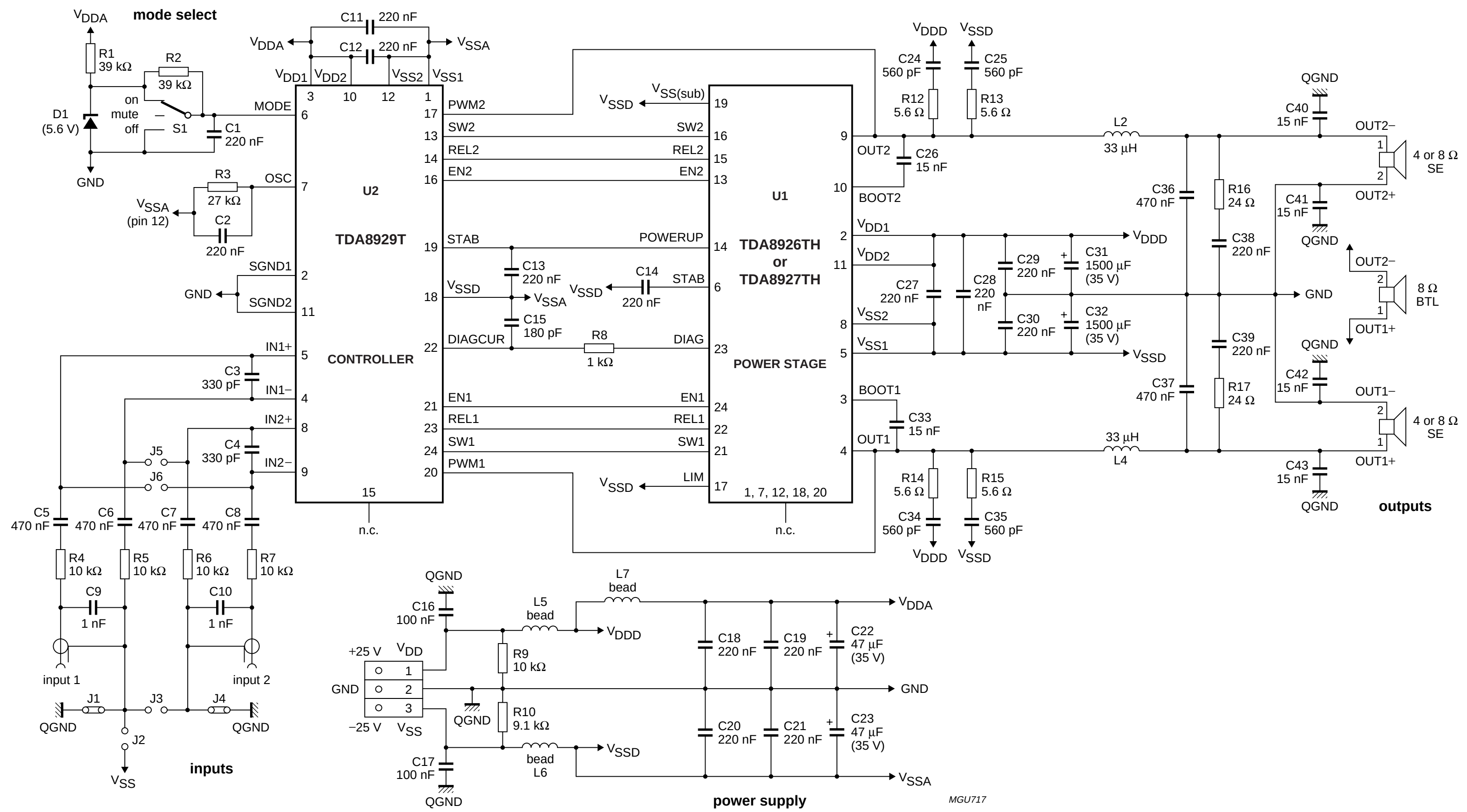
R_s = series resistance of filter coil

$P_{o(1\%)}$ = output power just at clipping

The output power at THD = 10%: $P_{o(10\%)} = 1.25 \times P_{o(1\%)}$.

15.4 Reference design

The reference design for a two-chip class-D audio amplifier for TDA8926TH and controller TDA8929T is shown in Fig.7.



Resistor R1 value $\leq \frac{V_{DD(min)} - 5.6\ V}{100\ \mu A}\ \Omega$.

Working voltage of SMD capacitors connected between V_{DD} and V_{SS} must be at least 63 V.

Capacitors C31 and C32 are electrolytic capacitors with low ESR.

Capacitors C36 and C37 are MKT types.

R9 and R10 are necessary only in BTL applications with asymmetrical supply.

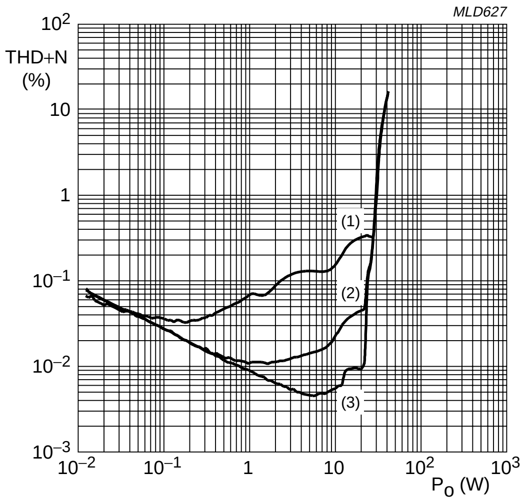
In BTL applications: remove input 2; remove R6, R7, C4, C7 and C8; close J5 and J6.

In BTL applications: demodulation coils L2 and L4 should be matched.

Inputs referred to QGND (close J1 and J4) or referred to V_{SS} (close J2 and J3).

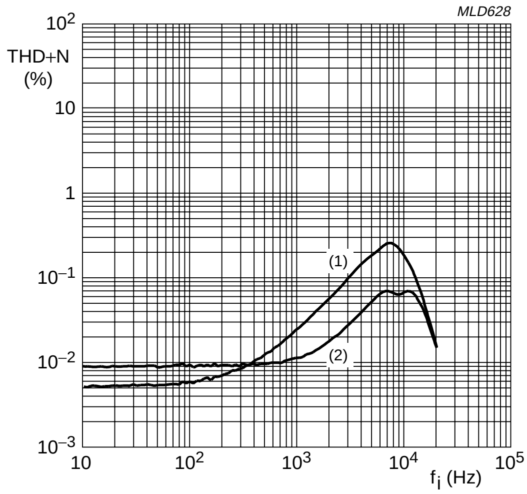
Fig.7 Two-chip class-D audio amplifier application diagram for TDA8926TH and controller TDA8929T.

15.5 Curves measured in reference design



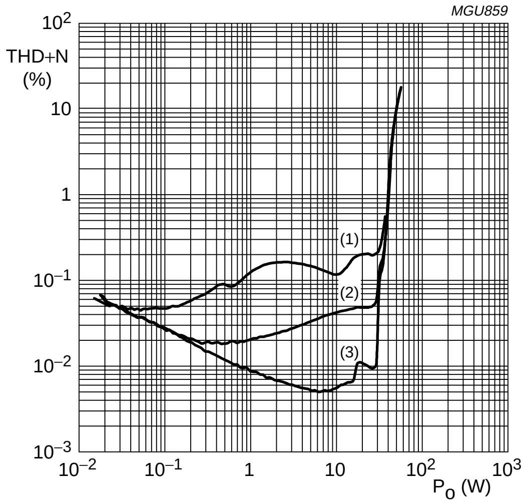
$2 \times 8\ \Omega$ SE; $V_P = \pm 25$ V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.8 Total harmonic distortion plus noise as a function of output power.



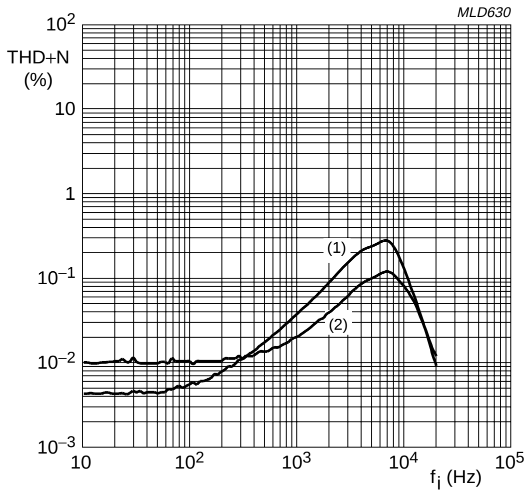
$2 \times 8\ \Omega$ SE; $V_P = \pm 25$ V.
(1) $P_o = 10$ W.
(2) $P_o = 1$ W.

Fig.9 Total harmonic distortion plus noise as a function of input frequency.



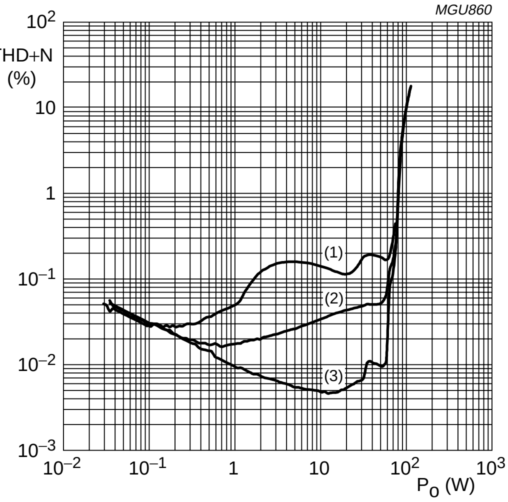
$2 \times 4\ \Omega$ SE; $V_P = \pm 21$ V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.10 Total harmonic distortion plus noise as a function of output power.



$2 \times 4\ \Omega$ SE; $V_P = \pm 21$ V.
(1) $P_o = 10$ W.
(2) $P_o = 1$ W.

Fig.11 Total harmonic distortion plus as a function of input frequency.



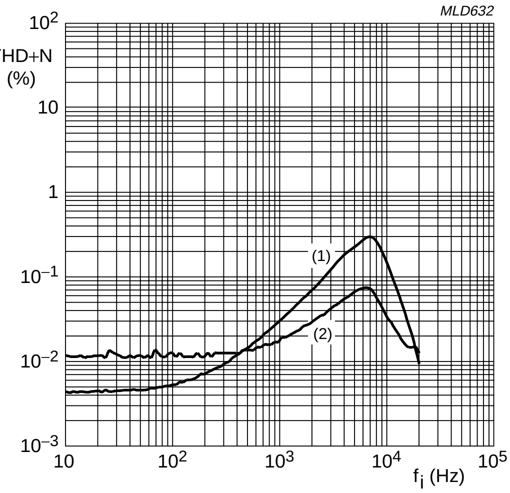
1 × 8 Ω BTL; V_P = ±21 V.

(1) 10 kHz.

(2) 1 kHz.

(3) 100 Hz.

Fig.12 Total harmonic distortion plus noise as a function of output power.

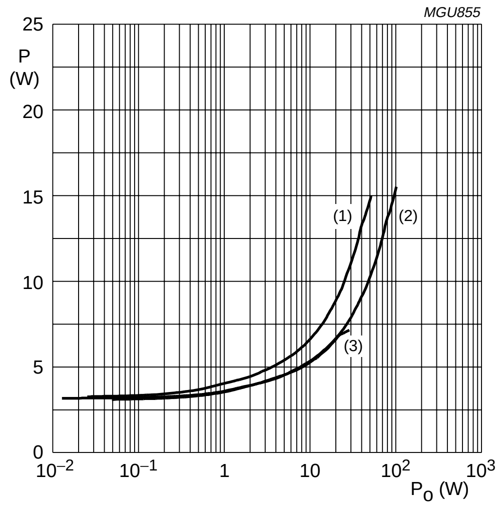


1 × 8 Ω BTL; V_P = ±21 V.

(1) P_o = 10 W.

(2) P_o = 1 W.

Fig.13 Total harmonic distortion plus noise as a function of input frequency.



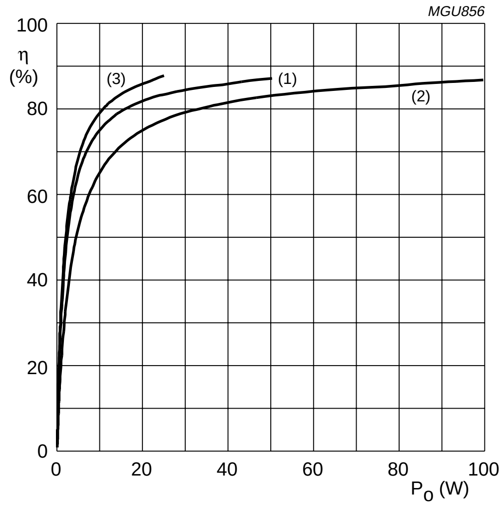
V_P = ±21 V; f_i = 1 kHz.

(1) 2 × 4 Ω SE.

(2) 1 × 8 Ω BTL.

(3) 2 × 8 Ω SE.

Fig.14 Power dissipation as a function of output power.



V_P = ±21 V; f_i = 1 kHz.

(1) 2 × 4 Ω SE.

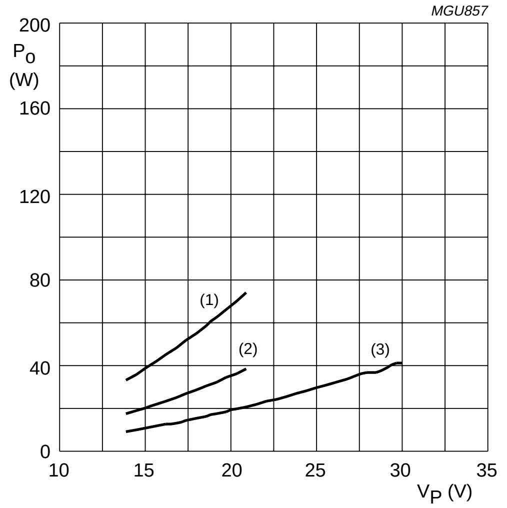
(2) 1 × 8 Ω BTL.

(3) 2 × 8 Ω SE.

Fig.15 Efficiency as a function of output power.

Power stage 2 × 50 W class-D audio amplifier

TDA8926TH



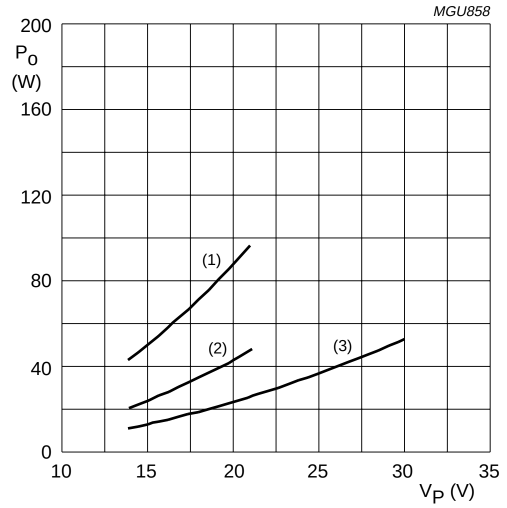
THD + N = 0.5%; f_i = 1 kHz.

(1) 1 × 8 Ω BTL.

(2) 2 × 4 Ω SE.

(3) 2 × 8 Ω SE.

Fig.16 Output power as a function of supply voltage.



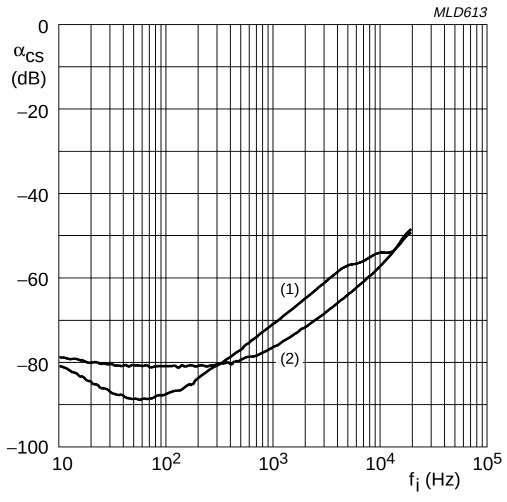
THD + N = 10%; f_i = 1 kHz.

(1) 1 × 8 Ω BTL.

(2) 2 × 4 Ω SE.

(3) 2 × 8 Ω SE.

Fig.17 Output power as a function of supply voltage.

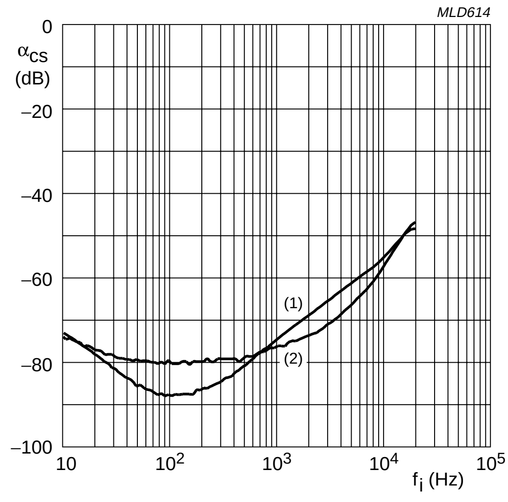


2 × 8 Ω SE; V_P = ±21 V.

(1) P_o = 10 W.

(2) P_o = 1 W.

Fig.18 Channel separation as a function of input frequency.

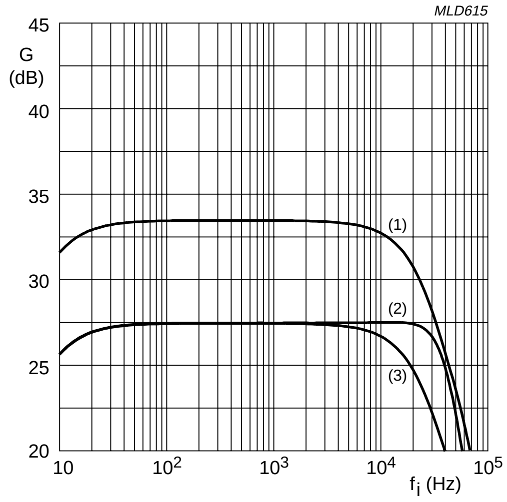


2 × 4 Ω SE; V_P = ±21 V.

(1) P_o = 10 W.

(2) P_o = 1 W.

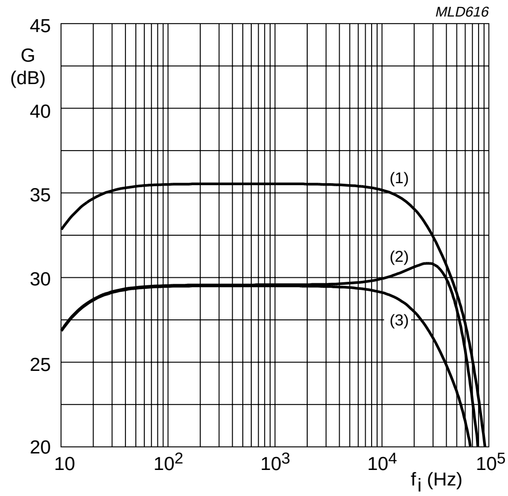
Fig.19 Channel separation as a function of input frequency.



V_P = ±21 V; V_i = 100 mV; R_s = 10 kΩ/C_i = 330 pF.

(1) 1 × 8 Ω BTL.
(2) 2 × 8 Ω SE.
(3) 2 × 4 Ω SE.

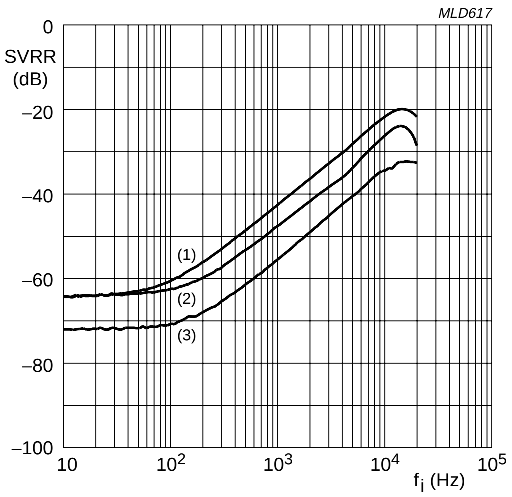
Fig.20 Gain as a function of input frequency.



V_P = ±21 V; V_i = 100 mV; R_s = 0 Ω.

(1) 1 × 8 Ω BTL.
(2) 2 × 8 Ω SE.
(3) 2 × 4 Ω SE.

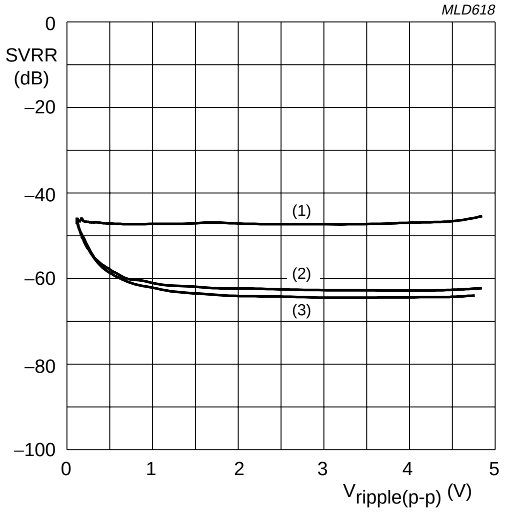
Fig.21 Gain as a function of input frequency.



V_P = ±21 V; $V_{ripple(p-p)}$ = 2 V.

(1) Both supply lines in antiphase.
(2) Both supply lines in phase.
(3) One supply line rippled.

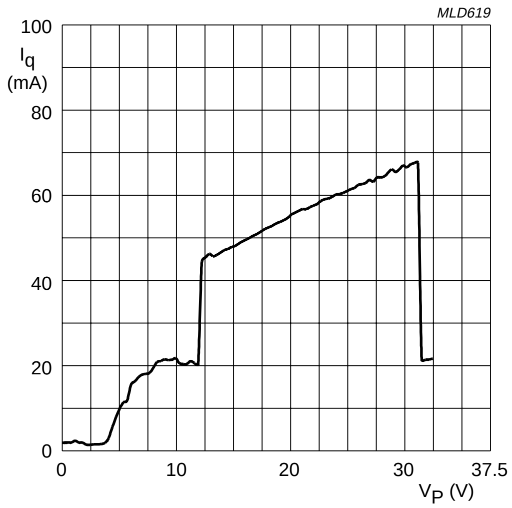
Fig.22 Supply voltage ripple rejection as a function of input frequency.



V_P = ±21 V.

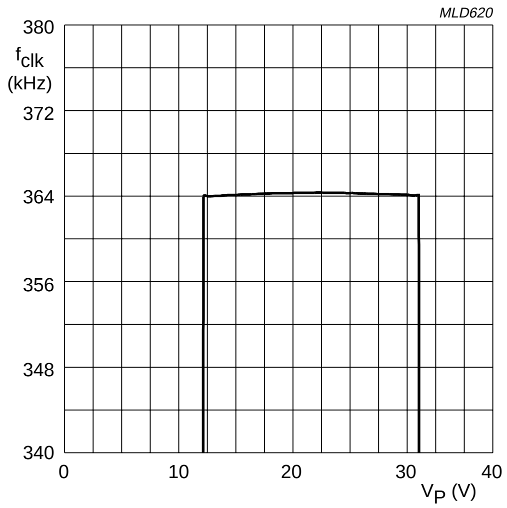
(1) f_{ripple} = 1 kHz.
(2) f_{ripple} = 100 Hz.
(3) f_{ripple} = 10 Hz.

Fig.23 Supply voltage ripple rejection as a function of ripple voltage (peak-to-peak value).



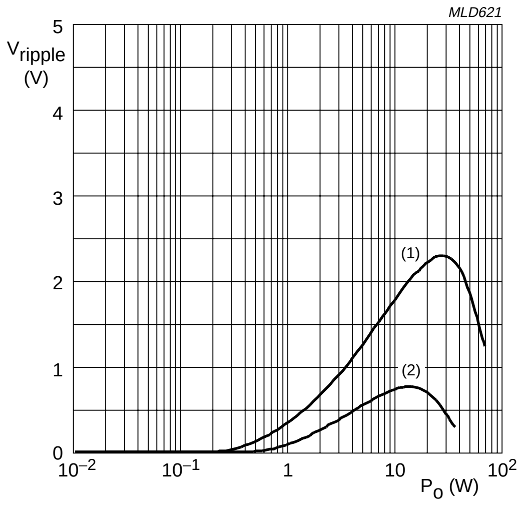
R_L = open-circuit.

Fig.24 Quiescent current as a function of supply voltage.



R_L = open-circuit.

Fig.25 Clock frequency as a function of supply voltage.

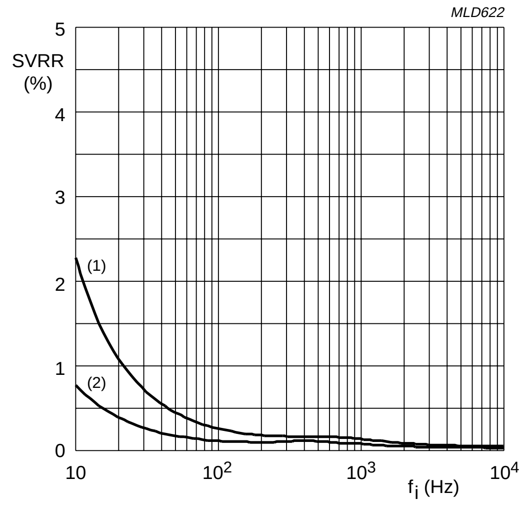


V_P = ±21 V; 1500 μF per supply line; f_i = 10 Hz.

(1) 1 × 4 Ω SE.

(2) 1 × 8 Ω SE.

Fig.26 Supply voltage ripple as a function of output power.

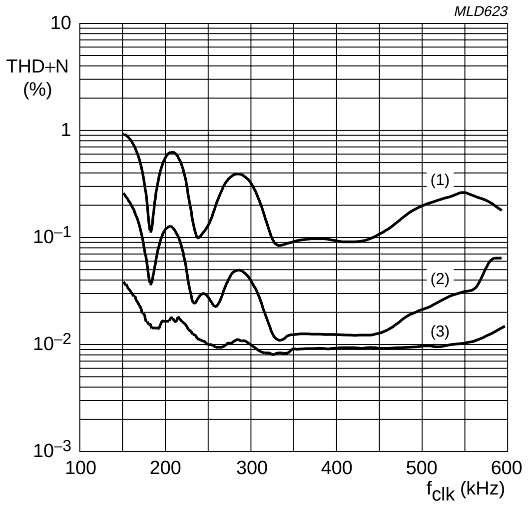


V_P = ±21 V; 1500 μF per supply line.

(1) P_o = 30 W into 1 × 4 Ω SE.

(2) P_o = 15 W into 1 × 8 Ω SE.

Fig.27 Supply voltage ripple rejection as a function of input frequency.



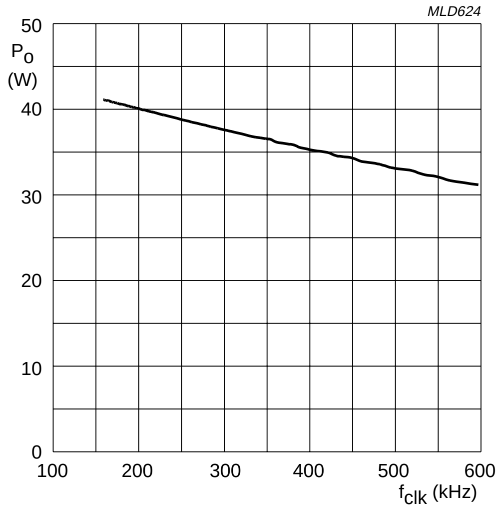
V_P = ±21 V; P_o = 1 W in 2 × 8 Ω.

(1) 10 kHz.

(2) 1 kHz.

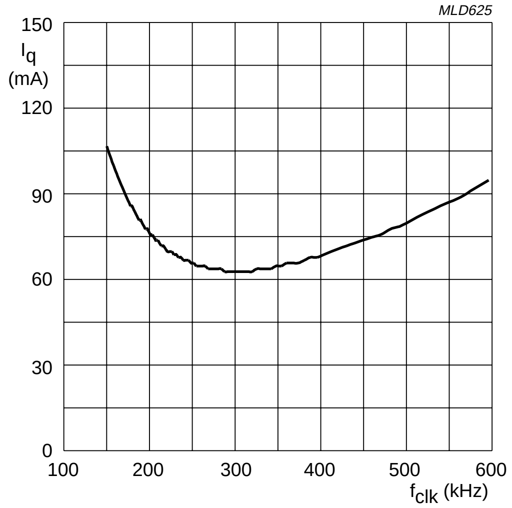
(3) 100 Hz.

Fig.28 Total harmonic distortion plus noise as a function of clock frequency.



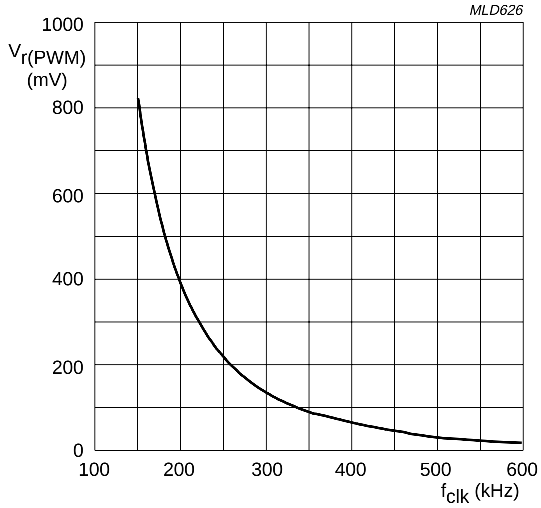
V_P = ±21 V; R_L = 2 × 8 Ω; f_i = 1 kHz; THD + N = 10%.

Fig.29 Output power as a function of clock frequency.



V_P = ±25 V; R_L = open circuit.

Fig.30 Quiescent current as a function of clock frequency.

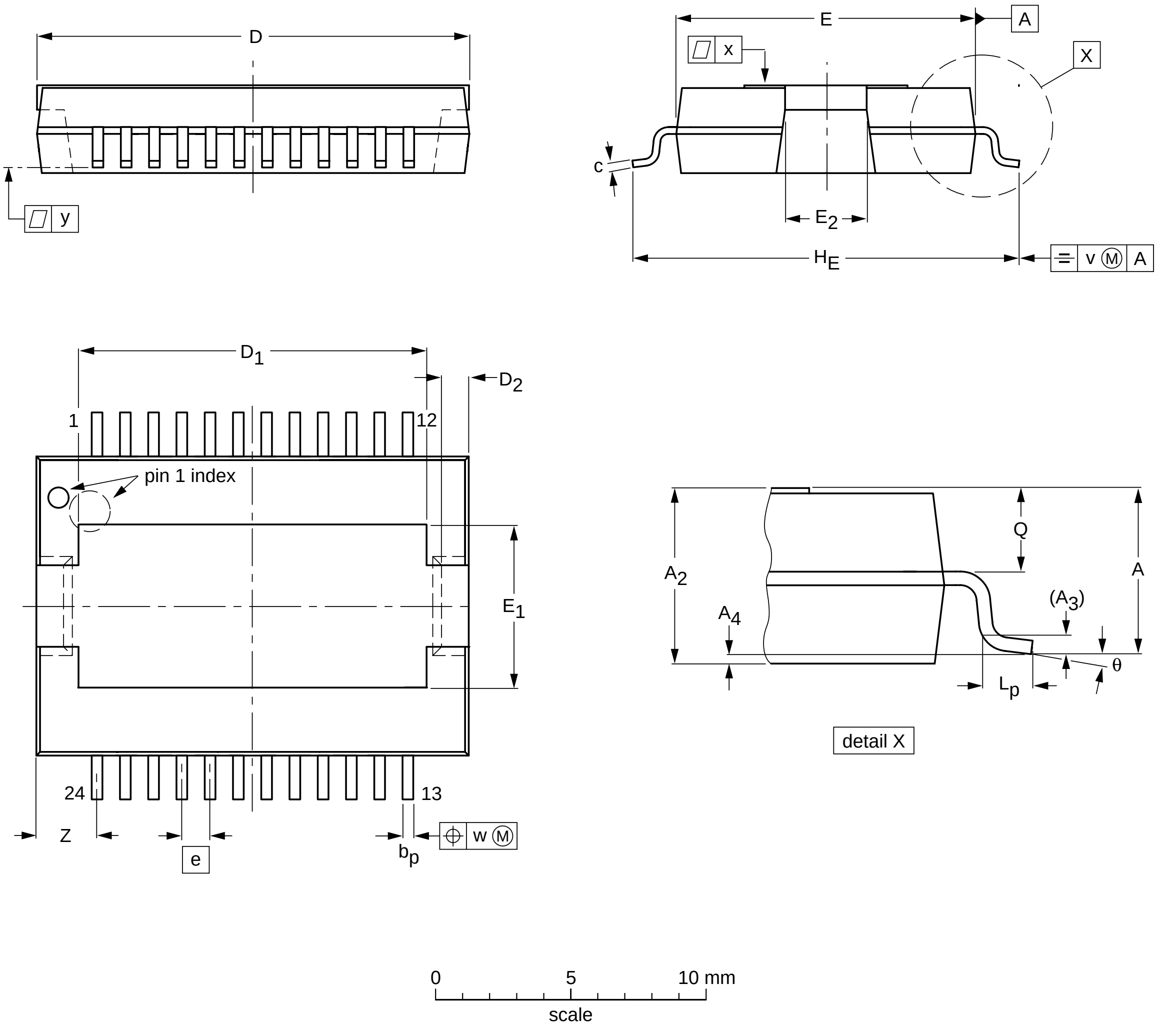


V_P = ±25 V; R_L = 2 × 8 Ω.

Fig.31 PWM residual voltage as a function of clock frequency.

16 PACKAGE OUTLINE

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						02-01-30

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[(1)]	PRODUCT STATUS[(2)(3)]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

20 DISCLAIMERS

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA74

Printed in The Netherlands 753503/02/pp28 Date of release: 2002 Oct 22 Document order number: 9397 750 09588

Let's make things better.

Philips
Semiconductors

PHILIPS