DATA SHEET

TDA9847
TV and VTR stereo/dual sound processor with digital identification

Preliminary specification
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Philips
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PHILIPS

TV and VTR stereo/dual sound processor with digital identification

TDA9847

FEATURES

- Supply voltage 5 to 8 V
- Source selector
- Stereo matrix
- AF inputs for external stereo AF signals (SCART or NICAM)
- AF outputs for main and SCART
- LED operation mode indication (stereo and dual)
- High identification reliability.

GENERAL DESCRIPTION

The TDA9847 is a stereo/dual sound processor for TV and VTR sets. Its identification ensures safe operation by using internal digital PLL technique with extremely small bandwidth, synchronous detection and digital integration (switching time maximum 2.0 s; identification concerning the main functions).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 22)		4.5	5	8.8	V
I_P	supply current (pin 22)	without LED current	14	15	20	mA
$V_{i(rms)}$	nominal input signal voltage V_{i1} to V_{i4} (RMS value)	54% modulation				
		B/G	–	250	–	mV
		L	–	500	–	mV
$V_{o(rms)}$	nominal output signal voltage (RMS value)	54% modulation	–	500	–	mV
$V_{o(rms)}$	clipping level of the output signal voltages (RMS value)	THD ≤ 1.5%; B/G or L				
		V_P = 5 V	1.4	1.60	–	V
		V_P = 8 V	2.4	2.65	–	V
I_{Lon}	input current	LED on	–	–	12	mA
$V_{i\ pil}$	input voltage sensitivity of pilot frequency	unmodulated	5	–	100	mV
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"*	66	75	–	dB
THD	total harmonic distortion		–	0.2	0.3	%
T_{amb}	operating ambient temperature		0	–	+70	°C
f_{ident}	identification window width	stereo	2.2	–	2.2	Hz
		dual	2.3	–	2.3	Hz
$t_{ident\ on}$	total identification time on		0.35	–	2.0	s
$V_{i\ tuner}$	identification voltage sensitivity		–	28	–	dBμV
Δf_{pil}	pull-in frequency range of pilot PLL	f_{osc} = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9847	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
TDA9847T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAMS

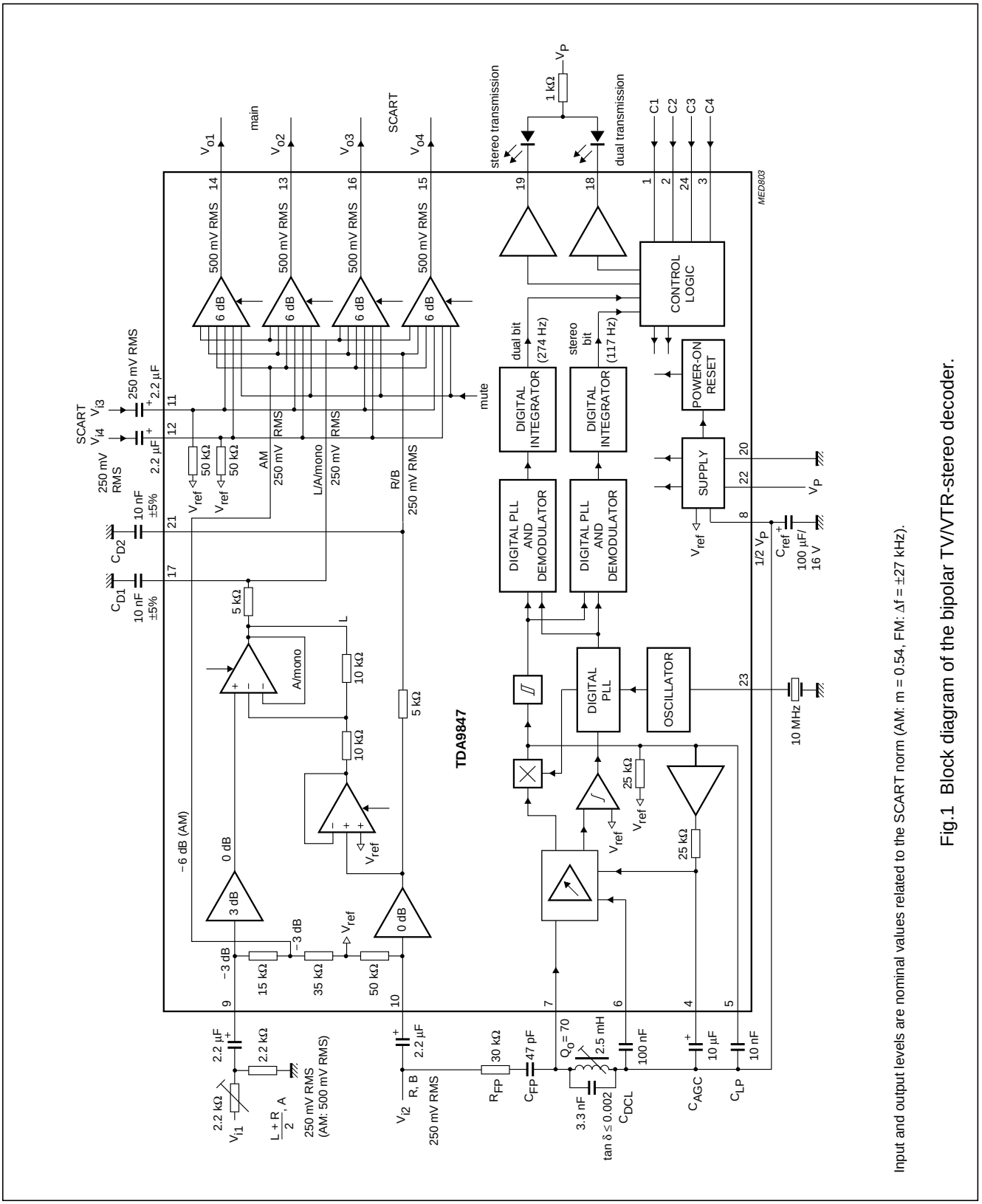


Fig.1 Block diagram of the bipolar TV/VTR-stereo decoder.

Input and output levels are nominal values related to the SCART norm (AM: m = 0.54, FM: Δf = ±27 kHz).

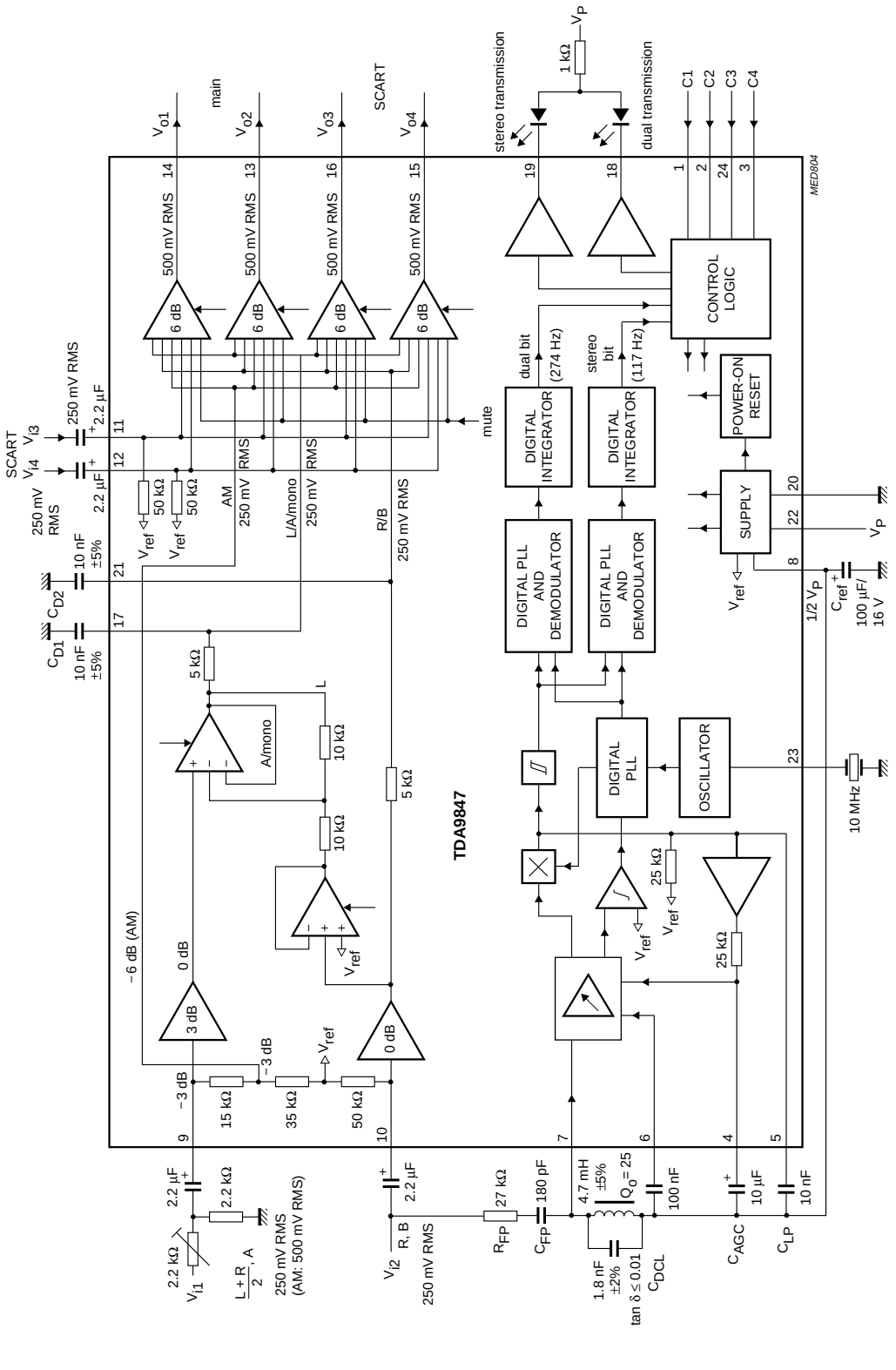


Fig.2 Block diagram of the bipolar TV/VTR-stereo decoder with fixed coil (alignment-free).

Input and output levels are nominal values related to the SCART norm (AM: m = 0.54, FM: Δf = ±27 kHz).
The components of the external LC band-pass filter have the following order-No.: Philips Germany only No: 4312 020 17525 or Fastron Sdn. Bha., Malaysia type SMCC 472 J for L = 4.7 MHz (±5%) Philips Components No: 2222 429 71802, C = 1.8 nF (±2%).

PINNING

SYMBOL	PIN	DESCRIPTION
C1	1	control input Port C1
C2	2	control input Port C2
C4	3	control input Port C4
C_{AGC}	4	AGC capacitor of pilot frequency amplifier
C_{LP}	5	identification low-pass capacitor
C_{DCL}	6	DC loop capacitor
$V_{i\ pil}$	7	pilot frequency input voltage
C_{ref}	8	capacitor of reference voltage ($\frac{1}{2}V_P$)
V_{i1}	9	AF input signal voltage 1 [from sound carrier 1 or AM sound (standard L)]
V_{i2}	10	AF input signal voltage 2 (from sound carrier 2)
V_{i3}	11	AF input signal voltage 3 (SCART)
V_{i4}	12	AF input signal voltage 4 (SCART)
V_{o2}	13	AF output signal voltage 2 (main)
V_{o1}	14	AF output signal voltage 1 (main)
V_{o4}	15	AF output signal voltage 4 (SCART)
V_{o3}	16	AF output signal voltage 3 (SCART)
C_{D1}	17	50 µs de-emphasis capacitor of AF Channel 1
LEDDU	18	LED (dual)
LEDST	19	LED (stereo)
GND	20	ground (0 V)
C_{D2}	21	50 µs de-emphasis capacitor of AF Channel 2
V_P	22	supply voltage (5 to 8 V)
XTAL	23	10 MHz crystal input
C3	24	control input Port C3

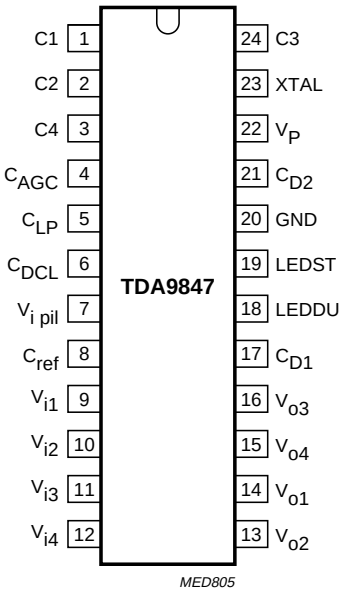


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

AF signal handling

The input AF signals, derived from the two sound carriers, are processed in analog form using operational amplifiers. De-matrixing uses the technique of two amplifiers processing the AF signals. Finally, a source selector provides the facility to route the mono signal through to the outputs ('forced mono').

De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. This provides a frequency response with the tolerances given in Fig.4.

A source selector, controlled via the control input ports allows selection of the different modes of operation in accordance with the transmitted signal. The device was designed for a nominal input signal (FM: 54% modulation is equivalent to $\Delta f = \pm 27$ kHz) of 250 mV RMS value (V_{i1} and V_{i2}) and for a nominal input signal (AM: m = 0.54) of 500 mV RMS value (V_{i1}), respectively 250 mV RMS (V_{i3} and V_{i4}). A nominal gain of 6 dB for V_{i1} and V_{i2} signals (0 dB for V_{i1} signal (AM sound)) and 6 dB for V_{i3} and V_{i4} signals is built-in. By using rail-to-rail operational amplifiers, the clipping level (THD $\leq$ 1.5%) is 1.60 V RMS for V_P = 5 V and 2.65 V RMS for V_P = 8 V at outputs V_{o1} to V_{o3} and V_{o4}. Care has been taken to minimize switching plops. Also total harmonic distortion and random noise are considerably reduced.

Identification

The pilot signal is fed via an external RC high-pass filter and single tuned LC band-pass filter to the input of a gain controlled amplifier. The external LC band-pass filter in combination with the external RC high-pass filter should have a loaded Q-factor of approximately 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil (±5%) to save the alignment (see Fig.2), a Q-factor of approximately 12 is proposed. This may cause a loss in sensitivity of approximately 2 to 3 dB. A digital PLL circuit generates a reference carrier, which is synchronized with the pilot carrier. This reference carrier and the gain controlled pilot signal are fed to the AM-synchronous demodulator. The demodulator detects the identification signal, which is fed through a low-pass filter with external capacitor CLP (pin 5) to a Schmitt trigger for pulse shaping and suppression of LOW level spurious signal components. This is a measure against mis-identification.

The identification signal is amplified and fed through an AGC low-pass filter with external capacitor CAGC (pin 4) to obtain the AGC voltage for controlling the gain of the pilot signal amplifier.

The identification stages consist of two digital PLL circuits with digital synchronous demodulation and digital integrators to generate the stereo or dual sound identification bits which can be indicated via LEDs.

A 10 MHz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_p-variations from the transmitter can be tracked in the event of missing synchronization with the horizontal frequency f_H. However the detection bandwidth for the identification signal is made small (±1 Hz) to reduce mis-identification.

Figure 2 shows an example of the alignment-free f_p band-pass filter. To achieve the required Q_L of around 12, the Q_0 at f_p of the coil was chosen to be around 25 (effective Q_0 including PCB influence). Using coils with other Q_0, the RC-network (R_{FP} and C_{FP}) has to be adapted accordingly. It is assumed that the loss factor tan δ of the resonance capacitor is $\leq$0.01 at f_p.

Copper areas under the coil might influence the loaded Q and have to be taken into account. Care has also to be taken in environments with strong magnetic fields when using coils without magnetic shielding.

Control input ports

The complete IC is controlled by the four control input ports C1, C2, C3 and C4. Which AF output channel pair can be selected is determined by the control input Port C4 [LOW: main; HIGH: SCART; 3-state: preset position (see Section "General information")]. With the other control input ports C1, C2 and C3 the user can select between different AF sources in accordance with the transmitter status (see Tables 1 and 2). Finally, Schmitt triggers are added in the input Port interfaces to suppress spikes on the control lines C1, C2, C3 and C4.

After a Power-On Reset (POR) both registers are reset (mute mode for both AF channel pairs). After some time ($\leq$1 ms), when the POR is automatically deactivated, the switch positions of the main channel (C4 = LOW) are changed in accordance with the other control input Port levels. If C4 is HIGH after a POR, the switch positions of the SCART channel cannot change. The reason is, that the main register is reset (mute mode; see Table 1). Thus, at first the main register byte has to be changed out of the mute function, e.g. sound mute.

After that, when C4 is HIGH (see Table 2), the switch positions of the SCART channel are changed in accordance with the other control line levels.

When the supply voltage of the TDA9847 is not connected (standby function), the control lines remain undisturbed.

The logic level combination 1000 of the control input ports (C4, C3, C2 and C1) is not allowed (see Tables 1 and 2).

Operating mode selection

Tables 1 and 2 show the different operating modes of this stereo decoder.

MUTE MODE

This IC has two different mute modes:

1. Mute mode.
2. Sound mute mode.

In the mute mode, when all control input lines are set LOW, all AF channels are muted ('fast mute'). Finally, the integrators are reset provided the user does not leave this mode (identification is disabled). When the user changes this mode, the identification circuit starts with the detection.

In the sound mute mode each AF channel can be separately muted (0100 = main and 1100 = SCART). The identification circuit is activated and the LEDs are on or off in accordance with the detection status of this circuit.

MONO MODE

For the transmitter status mono the user must set the TDA9847 in the mono mode with X001 or X010 (see Tables 1 and 2). The level combination X011 is reserved for the AM sound (standard L), because in this mode the de-emphasis is deactivated and the gain of the AF signal from input to output is reduced from 6 dB to 0 dB. At the AF outputs the signal has the same level for standards with FM or AM modulated sound assuming the same modulation degree.

STEREO MODE

In this mode the choice between stereo and mono ('forced mono') signals is common for both AF channel pairs. The mode for main and SCART is achieved by control of the main channel (see Tables 1 and 2).

DUAL MODE

In this mode there is no restriction to select AF inputs and outputs independently in both channels.

EXTERNAL MODE

External sound sources, e.g. from SCART input, are fed to both AF channel pair outputs. When the user chooses the external mode of the main channel (see Table 1), the identification circuit is still running, but the LEDs are switched-off.

Programming of the main and SCART register

GENERAL INFORMATION

The switch positions of both AF channels are directly controlled by the data of the main and SCART register. These registers are programmable by a microcontroller.

In the 3-state mode the logic content of the C1, C2 and C3 control lines remains stored in the registers for main and SCART, so the switch positions in the source selector do not change. The logic content of these control lines can be changed without changing the switch positions of the source selector (preset position) to prepare the new operating mode selection for the main or SCART channel. The execution of this new mode is achieved by leaving the preset position (3-state): When the C4 level goes LOW, the logic content of the control lines C1, C2 and C3 are valid for the main channel (see Table 1) and in the event of HIGH the C1, C2 and C3 are valid for the SCART channel (see Table 2).

The identification bits and the control lines influence the operating mode selection for the AF switches in the source selector and de-matrix, e.g. both AF channels are programmed in the mono mode (X001, see Tables 1 and 2). The LEDs are switched-off. When the identification circuit detects the stereo identification frequency (f_s = 117 Hz) the de-matrix is immediately switched in the stereo mode without changing the control line levels. The stereo signals are routed to all AF outputs. In the event of dual frequency detection (f_D = 274 Hz) both dual sounds are fed to the AF output pairs.

MICROCONTROLLER WITH 3-STATE OUTPUT PORTS

Figure 10 shows an example of an application circuit for TDA9847 (V_P = 4.5 to 8.8 V) in conjunction with a microcontroller, which has a LOW/high-ohmic/HIGH output port to control the main and SCART channel (C4 control line). For the C1, C2 and C3 line the microcontroller requires only LOW/HIGH output ports. Two resistors R_{C4A} and R_{C4B} are necessary for the C4 line to generate the 3-state voltage. The values and tolerances of these components are given in Fig.10.

When the microcontroller has only open drain ports available for the C1, C2 and C3 control line, external pull-up resistors must be connected to these control lines.

Figure 7 shows an example of a timing diagram to program the main and SCART register of the TDA9847 with a microcontroller via the control lines C1, C2, C3 and C4. Both registers are programmed with the same control line levels: C1 = LOW, C2 = HIGH and C3 = LOW. The dual identification frequency is detected and the dual LED is switched-on. The A-signal (dual mode) is fed to all AF outputs (see Tables 1 and 2). This is shown in the beginning of this timing diagram.

The second period of time shows the programming of the external mode (C3 goes to HIGH: CC-signal) for the main channel. The switch positions are immediately changed to the external AF source, because the C4 level is LOW. The dual LED is switched-off by the logic (see Section “External mode”).

The next periods of time show the way to change the switch positions for the SCART channel to route B-signals to the AF outputs (dual mode: BB). At first the control output Port of the microcontroller for the C4 line goes into the high ohmic state. The changing of the C1, C2 or C3 level has no influence on the register data. In the timing diagram the C1 level changes from LOW-to-HIGH and the C3 level goes from HIGH-to-LOW. In the next steps the C4 line goes from 3-state-to-HIGH, and the level of the other control lines are valid for the SCART channel, and the B-signals are fed (dual mode: BB) to the AF outputs of the main channel.

After some time in this example the C1 and C2 levels change from HIGH-to-LOW and the C3 level goes from LOW-to-HIGH (sound mute). The SCART channel is immediately muted, because the level of the C4 line is HIGH.

The last period of time shows the programming of the dual mode (AA) for the main channel. At first the control output Port of the microcontroller for the C4 line goes into the high ohmic state. The changing of the C1, C2 or C3 level has no influence on the register data. The switch positions of the SCART channel stay in the sound mute.

In the 3-state mode the C2 level changes from LOW-to-HIGH, and the C3 level goes from HIGH-to-LOW. When the C4 level is LOW, the level of the other control lines are valid for the main channel. The A-signal (dual mode) is fed to the main outputs.

The operation mode mute (see Table 1) can be achieved from any position of the C4 control line without going via 3-state.

Figure 5 shows the hold and set-up time of the C1, C2 and C3 control line in the 3-state mode, see Chapter “Characteristics”.

MICROCONTROLLER WITH LOW/HIGH OUTPUT PORTS

Figure 11 shows an example of an application circuit for TDA9847 (V_P = 4.5 to 8.8 V) in conjunction with a microcontroller, which has open drain output ports to control the main and SCART channel. Four resistors and two output ports of the microcontroller are necessary to generate the 3-state voltage. The other control lines have a pull-up resistor (10 kΩ) in the event of open drain output stages. These resistors are not necessary for LOW/HIGH output ports of the microcontroller having internal pull-up or push-pull stages. The values and tolerances of these components are given in this figure. Table 4 shows the conversion logic truth table.

For information about programming the different operation mode selections see Section “Operating mode selection”.

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from an internal band-gap reference circuit. The AF reference voltage is $\frac{1}{2}V_P$. For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added. A good ripple rejection is achieved with the external capacitor C_{ref} = 100 µF/16 V in conjunction with the high ohmic input of the $\frac{1}{2}V_P$ pin (pin 8). No additional DC load on this pin is allowed.

Power-On Reset (POR)

When a POR is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117/274 Hz DPLL, the 117/274 Hz integrator and the logic will be reset. Both AF channels (main and SCART) are muted (≤1 ms).

ESD protection

All pins are ESD protected. The protection circuits represent the latest state of the art.

Internal circuit

The internal pin configuration is given in Fig.7.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 22)		–0.3	+10	V
V_i	input voltage at pins 1 to 3 and 24		–0.3	+9.0	V
V_i	input voltage at pins 4 to 17, 21 and 23		–0.3	V_P	V
V_i	input voltage at pins 18 and 19		–0.3	+10	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{es}	electrostatic handling for all pins	note 1	–	±300	V

Note

1. Charge device model class B: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP24	69	K/W
	SO24	95	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; nominal input signal $V_{i1,\ 2}$ = 0.25 V RMS value (FM: 54% modulation is equivalent to Δf = ±27 kHz); nominal input signal V_{i1} = 0.5 V RMS value (AM: m = 0.54); nominal input signal $V_{i3,\ 4}$ = 0.25 V RMS value (AM: m = 0.54); nominal output signal $V_{o1,\ 2,\ 3,\ 4}$ = 0.5 V RMS value; f_{AF} = 1 kHz; $V_{i\ pil}$ = 16 mV RMS value; f_{pil} = 54.6875 kHz (identification frequencies: stereo = 117.48 Hz, dual = 274.12 Hz), 50 µs pre-emphasis; noise measurement in accordance with *"CCIR468-3"*, operating oscillator frequency f_{osc} = 10.008 MHz; currents into the IC positive; measured in test circuit Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 22)		4.5	5	8.8	V
I_P	supply current (pin 22)	without LED current	14	15	20	mA
P_{tot}	total power dissipation		63	75	176	mW
$V_{n(DC)}$	DC voltage (pins 9 to 17 and 21)		$\frac{1}{2}V_P$ – 0.1	$\frac{1}{2}V_P$	$\frac{1}{2}V_P$ + 0.1	V
$V_{ref(DC)}$	DC reference voltage (pin 8)		$\frac{1}{2}V_P$ – 0.1	$\frac{1}{2}V_P$	$\frac{1}{2}V_P$ + 0.1	V
$I_{L(DC)}$	DC leakage current (pin 8)		–	–	±1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF Inputs (V_{i1} and V_{i2} [pins 9 and 10)]						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation				
		B/G	–	0.25	–	V
		L (only V_{i1})	–	0.5	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤1.5%				
		V_P = 5 V; B/G	0.625	0.715	–	V
		V_P = 8 V; B/G	1.050	1.200	–	V
		V_P = 5 V; L (only V_{i1})	1.200	1.400	–	V
		V_P = 8 V; L (only V_{i1})	2.100	2.350	–	V
G_v	AF signal voltage gain	G = V_o/V_i; note 1				
		B/G	5	6	7	dB
		L (only V_{i1})	–1	0	+1	dB
R_i	input resistance		40	50	60	kΩ
R_{deem}	internal de-emphasis resistor (pins 17 and 21)	see Fig.4	4.25	5.0	5.75	kΩ
Additional AF inputs (pins 11 and 12)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.25	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	0.625	0.715	–	V
		V_P = 8 V	1.050	1.200		V
G_v	AF signal voltage gain	G = V_o/V_i; note 1	5	6	7	dB
R_i	input resistance		40	50	60	kΩ
AF outputs (pins 13 to 16)						
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤ 0.3%; 54% modulation	–	0.5	–	V
$V_{o(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
R_o	output resistance		250	350	450	Ω
C_L	load capacitor on output		–	–	1.5	nF
R_L	load resistor on output (AC-coupled)		10	–	-	kΩ
B	frequency response (bandwidth)	f_i = 40 to 20000 Hz; note 2	–0.5	–	+0.5	dB
$B_{-3\ dB}$	frequency response	–3 dB; note 2	300	350	400	kHz
THD	total harmonic distortion	note 1	–	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"* (quasi-peak)	66	75	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cr}	crosstalk attenuation for	notes 1 and 3				
	dual	$\lvert Z_s \rvert \leq 1$ kΩ	70	75	–	dB
	stereo	$\lvert Z_s \rvert \leq 1$ kΩ	40	45	–	dB
α_{mute}	mute attenuation	$\lvert Z_s \rvert \leq 1$ kΩ; note 1	76	80	–	dB
ΔV_{DC}	change of DC level output voltage between any two modes of operation	after switching	–	–	±10	mV
PSRR	power supply ripple rejection	f_r = 70 Hz; see Fig.9	50	65	–	dB
$I_{O(DC)}$	DC output current		–	–	±20	µA
10 MHz crystal oscillator (pin 23)						
f_r	series resonant frequency of crystal (fundamental mode)	C_L = 20 pF	9.995	10.008	10.021	MHz
f_{osc}	operating oscillator frequency (running in parallel resonance mode)	over operating temperature range including ageing and influence of drive circuit	9.988	10.008	10.028	MHz
R_{xtal}	equivalent crystal series resistance	even at extremely low drive level (<1 pW) over operating temperature range with C_0 = 6 pF	–	60	200	Ω
R_n	crystal series resistance of unwanted mode		$2 \times R_r$	–	–	Ω
C_0	crystal parallel capacitance	with $R_r \leq 100$ Ω	–	6	10	pF
C_1	crystal motional capacitance		–	25	50	fF
P_{xtal}	level of drive in operation		–	–	5	µW
$V_{osc(p-p)}$	oscillator operating voltage (peak-to-peak value)		500	550	600	mV
Pilot processing						
$V_{i\ pil(rms)}$	pilot input voltage level at pin 7 (RMS value)	unmodulated	5	–	100	mV
$R_{i\ pil}$	pilot input resistance		500	1000	–	kΩ
$C_{i\ pil}$	pilot input capacitance		–	–	3	pF
m	modulation depth	AM	25	50	75	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δf_{pil}	pilot PLL pull-in frequency range (referenced to f_{pil} = 54.6875 kHz)	f_{osc} = 9.988 MHz				
		lower side	–405	–	–405	Hz
		upper side	192	–	192	Hz
		f_{osc} = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz
		f_{osc} = 10.028 MHz				
		lower side	–188	–	–188	Hz
		upper side	411	–	411	Hz
t_{pil}	pilot PLL pull-in time		0	–	1.7	ms
f_{LP}	low-pass frequency response	–3 dB	450	600	750	Hz
R_5	low-pass output resistance		18.75	25	31.25	kΩ
$V_{5(rms)}$	identification threshold voltage (RMS value)		–	–	70	mV
Q_L	loaded quality factor of resonance circuit	high sensitivity; see Fig.1	40	–	50	
	loaded quality factor of resonance circuit with fixed coil	sensitivity loss 2 to 3 dB; see Fig.2	–	12	–	
$t_{acqui\ AGC}$	AGC acquisition time	$V_{i\ pil(rms)}$ switched from 0 to 100 mV (RMS value)	–	–	0.1	s
Identification (internal functions)						
$V_{i\ tuner}$	identification voltage sensitivity	note 4	–	28	–	dBμV
C/N	pilot carrier-to-noise ratio for start of identification	note 5	–	33	-	dB/Hz
H	hysteresis	note 4	–	–	2	dB
f_{det}	pull-in frequency range of identification PLL (referred to $f_{det\ stereo}$ = 117.48 Hz and $f_{det\ dual}$ = 274.12 Hz)	lower side				
		stereo	–0.63	–	–0.63	Hz
		dual	–0.69	–	–0.69	Hz
		upper side				
		stereo	0.63	–	0.63	Hz
		dual	0.69	–	0.69	Hz
t_{det}	pull-in time of identification PLL (referenced to $f_{det\ stereo}$ = 117.48 Hz and $f_{det\ dual}$ = 274.12 Hz)	stereo	0	–	0.8	s
		dual	0	–	0.8	s
f_{ident}	identification window frequency width (referred to $f_{det\ stereo}$ = 117.48 Hz and $f_{det\ dual}$ = 274.12 Hz)	stereo; note 6	2.2	–	2.2	Hz
		dual; note 6	2.3	–	2.3	Hz
t_{integr}	integrator time constant		0.94	–	0.94	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{ident(on)}$	total identification time on	stereo; note 7	0.35	–	2.0	s
		dual; note 7	0.35	–	2.0	s
$t_{ident(off)}$	total identification time off	stereo; note 8	0.60	–	1.5	s
		dual; note 8	0.60	–	1.5	s
LED (pins 18 and 19)						
$V_{L(off)}$	output voltage	LED off	–	–	8.8	V
$V_{L(on)}$	output voltage	LED on	–	–	0.7	V
$I_{L(off)}$	input current	LED off	–	–	1	µA
$I_{L(on)}$	input current	LED on	–	–	12	mA
Control input ports C1 to C3 (pins 1, 2 and 24)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	5.0	8.8	V
I_{IL}	LOW level input current		–	–	-1	µA
I_{IH}	HIGH level input current		–	–	1	µA
Control input Port C4 (pin 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{CT}	3-state level input voltage		1.5	1.8	2.1	V
V_{IH}	HIGH level input voltage		2.8	5.0	8.8	V
I_{IL}	LOW level input current		–	–	–1	µA
I_{CT}	3-state level input current		–	–	–1	µA
I_{IH}	HIGH level input current		–	–	1	µA
t_{h1}	HIGH level hold time	see Fig.5	5	–	–	µs
t_{h2}	LOW level hold time	see Fig.5	5	–	–	µs
t_{su1}	HIGH level set-up time	see Fig.5	0.25	–	–	µs
t_{su2}	LOW level set-up time	see Fig.5	0.25	–	–	µs

Notes to the characteristics

1. V_o = 0.5 V (RMS value); f = 1 kHz.
2. Without de-emphasis capacitors with respect to nominal gain.
3. In dual mode: A (B)-signal into B (A) channel; in stereo mode: R-signal into left channel; L-signal = 0.
4. Tuner input signal, measured with PCALH reference front end (½EMF, 75 Ω, 2T/20T/white bar, 100% video) and PC/SC_1 = 13 dB; PC/SC_2 = 20 dB. The pilot band-pass has to be aligned.
5. Bandwidth of the pilot BP-filter $B_{-3\ dB}$ = 1.2 kHz. V_{i2} input driven with identification-modulated pilot carrier and white noise.
6. Identification window is defined as twice the pull-in frequency range (lower plus upper side) of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).
7. The maximal total system identification time on is equal to $t_{ident(on)}$ plus $t_{acqui\ AGC}$.
8. The maximal total system identification time off is equal to $t_{ident(off)}$.

Table 1 Control input Port matrix to select AF inputs and AF outputs (main channel)

MODE		INPUT SIGNAL				OUTPUT SIGNAL				CONTROL INPUT PORT(1)				LED	
		ST/DS/M		SCART		MAIN		SCART							
		V_{i1} 9	V_{i2} 10	V_{i3} 11	V_{i4} 12	V_{o1} 14	V_{o2} 13	V_{o3} 16	V_{o4} 15	C4 3	C3 24	C2 2	C1 1	DUAL 18	STEREO 19
Mute(2)	–	–	–	–	–	no signal		no signal		0	0	0	0	off	off
Sound mute	–	–	–	–	–	no signal		note 3		0	1	0	0	note 4	note 4
Mono	M	M	–	–	–	M	M	note 3		0	0	0	1	off	off
		M	–	–	–	M	M			0	0	1	0	off	off
		AM	–	–	–	AM	AM			0	0	1	1	off	off
Stereo	ST	S	R	–	–	L	R	L	R	0	0	0	1	off	on
		S	R	–	–	S	S	S	S	0	0	1	0	off	on
		S	R	–	–	S	S	S	S	0	0	1	1	off	on
Dual	DS	A	B	–	–	A	B	note 3		0	0	0	1	on	off
		A	B	–	–	A	A			0	0	1	0	on	off
		A	B	–	–	B	B			0	0	1	1	on	off
External	–	–	–	C	D	C	D	note 3		0	1	0	1	off	off
		–	–	C	D	C	C			0	1	1	0	off	off
		–	–	C	D	D	D			0	1	1	1	off	off

Notes

1. The combination 1000 is not allowed.
2. In mute mode the content of the 117 Hz/274 Hz integrator will be reset. The LEDs are switched-off.
3. The previous state is unchanged.
4. The LED shows the identification status.

Table 2 Control input Port matrix to select AF inputs and AF outputs (SCART channel)

MODE		INPUT SIGNAL				OUTPUT SIGNAL				CONTROL INPUT PORT(1)			
		ST/DS/M		SCART		MAIN		SCART					
		V_{i1} 9	V_{i2} 10	V_{i3} 11	V_{i4} 12	V_{o1} 14	V_{o2} 13	V_{o3} 16	V_{o4} 15	C4 3	C3 24	C2 2	C1 1
Sound mute	–	–	–	–	–	note 2		no signal		1	1	0	0
Mono	M	M	–	–	–	note 2		M	M	1	0	0	1
		M	–	–	–			M	M	1	0	1	0
		AM	–	–	–			AM	AM	1	0	1	1
Stereo	ST	S	R	–	–	note 2		–	–	1	0	0	1
		S	R	–	–			–	–	1	0	1	0
		S	R	–	–			–	–	1	0	1	1
Dual	DS	A	B	–	–	note 2		A	B	1	0	0	1
		A	B	–	–			A	A	1	0	1	0
		A	B	–	–			B	B	1	0	1	1
External	–	–	–	C	D	note 2		C	D	1	1	0	1
		–	–	C	D			C	C	1	1	1	0
		–	–	C	D			D	D	1	1	1	1

Notes

1. The combination 1000 is not allowed.
2. The previous state is unchanged.

Table 3 Explanation of Tables 1 and 2

SIGNAL	DESCRIPTION
R	right
L	left
S	$\frac{(L+R)}{2}$
A and B	dual sound A/B
C and D	external sound source (SCART)
AM	AM sound (standard L)
M	mono sound
DS	dual sound
ST	stereo sound

Table 4 Conversion logic truth table for the C4 control line (see Fig.11)

MICROPROCESSOR OUTPUT CONTROL PORTS		TDA9847	
C41	C42	C4	C4-level
0	0	1	≥3.2 V
1	0	3-state	1.8 ±0.25 V
1	1	0	≤0.45 V
0	1	not allowed	undefined

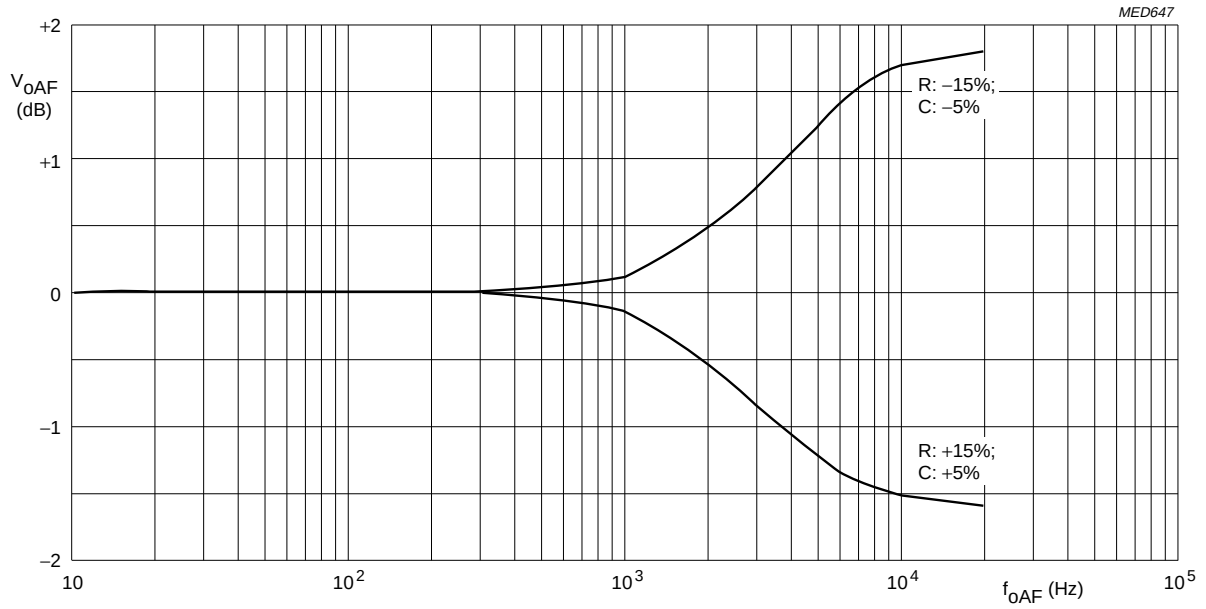


Fig.4 Tolerance scheme of AF frequency response; de-emphasis with C_{D1}, C_{D2} = 10 nF (±5%); $R_{internal}$ = 5 kΩ (±15%).

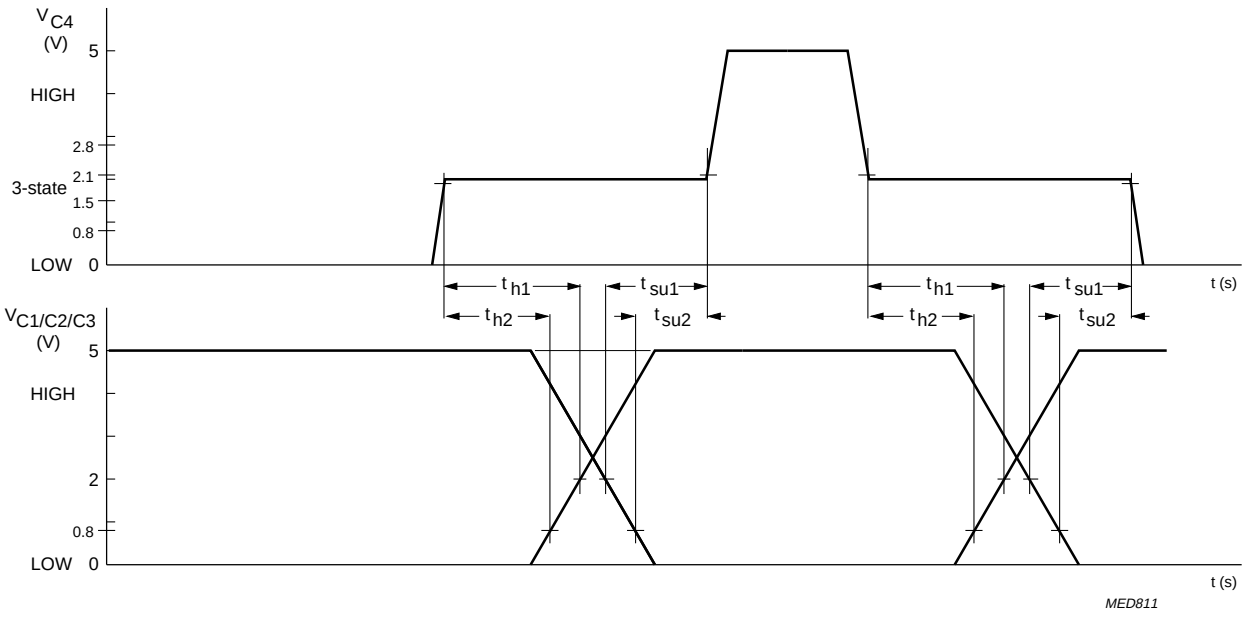


Fig.5 Waveforms showing the hold and set-up times of the C1 to C3 control line in the 3-state mode.

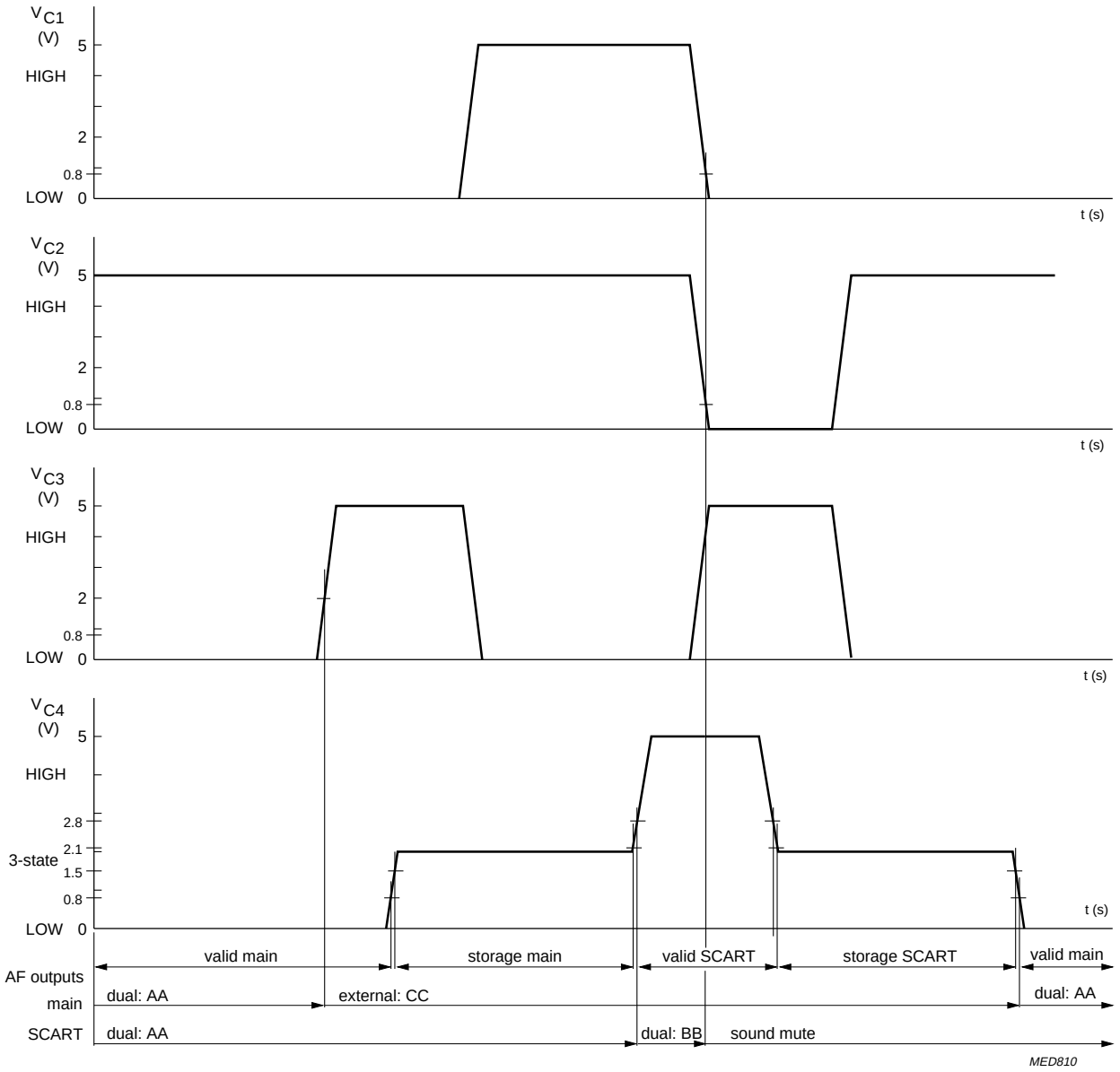


Fig.6 Programming the main and SCART register of the TDA9847 with a microcontroller via the control lines C1 to C4; the dual identification frequency is detected.

INTERNAL CIRCUITRY

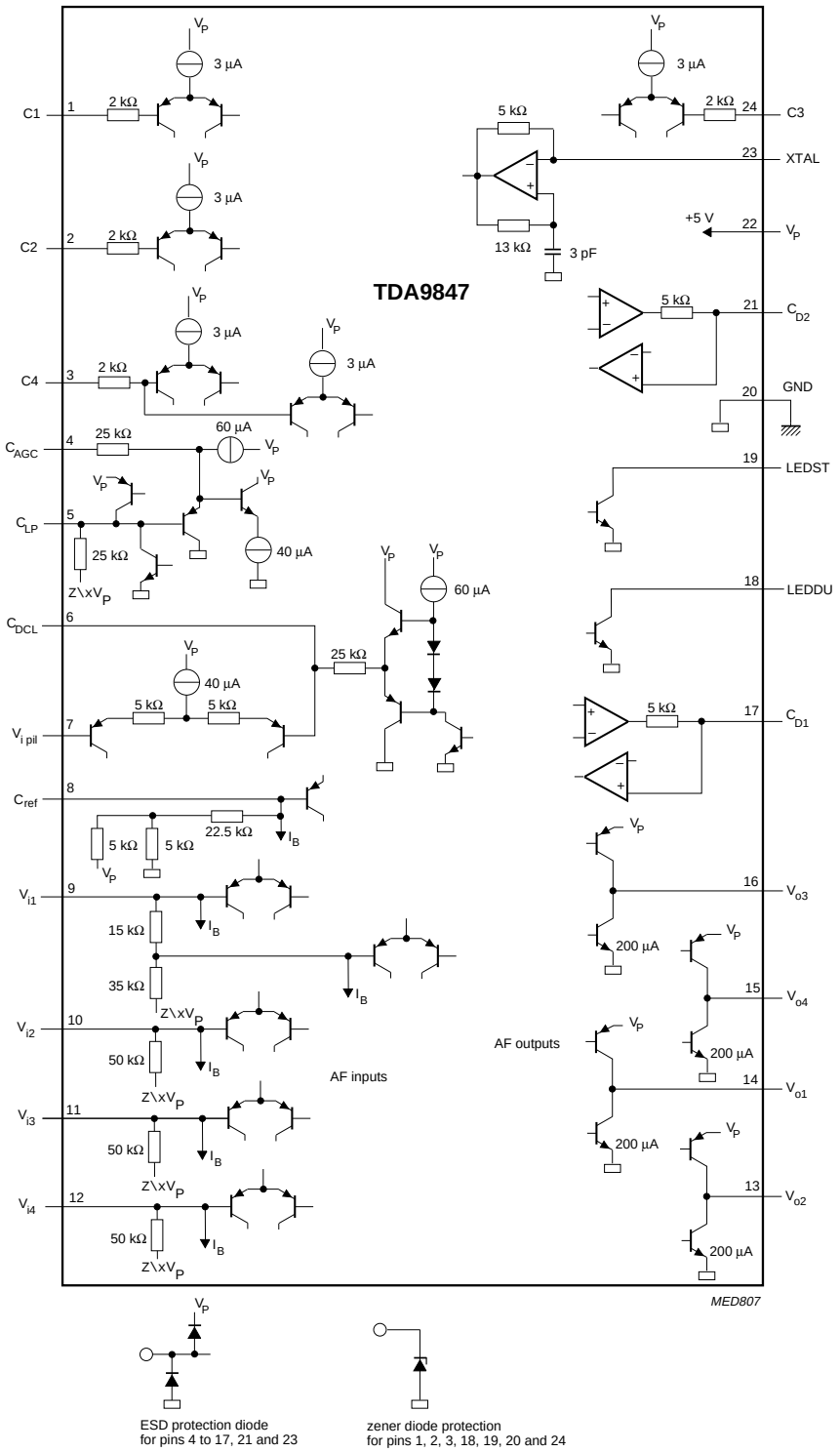


Fig.7 Internal circuits.

TEST AND APPLICATION INFORMATION

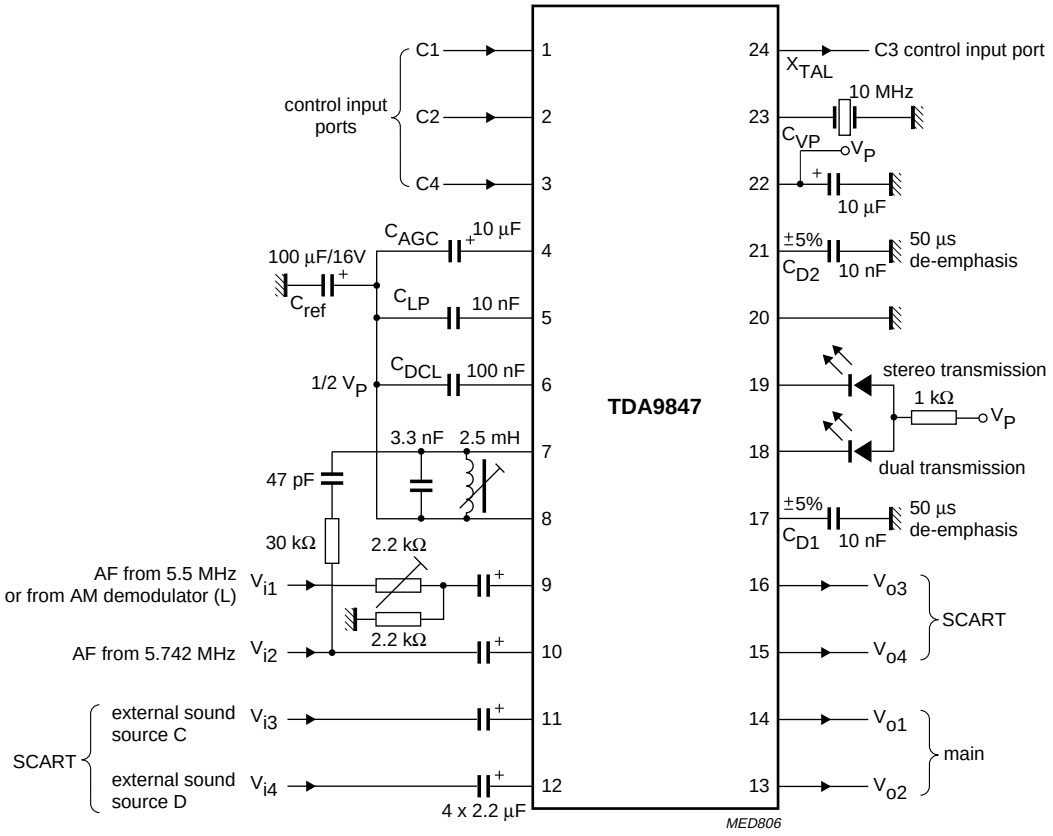


Fig.8 Test circuit of the stereo decoder TDA9847.

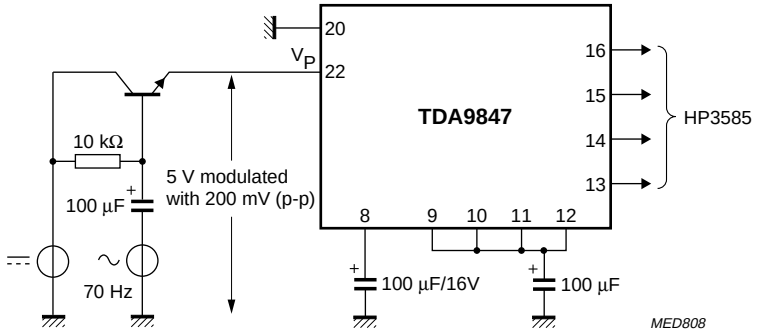
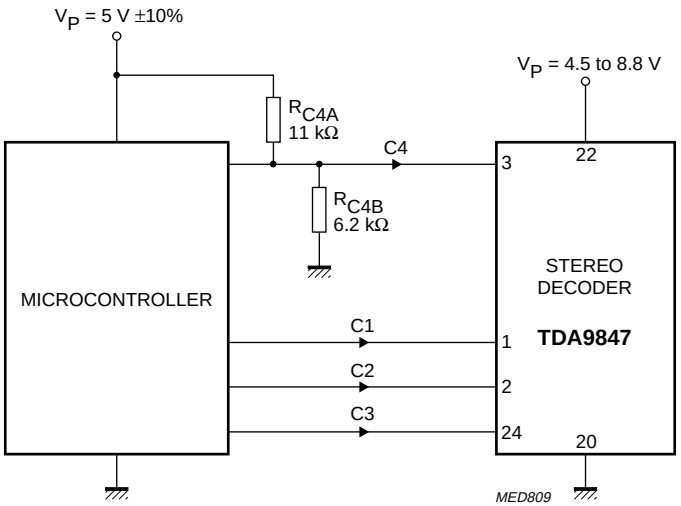
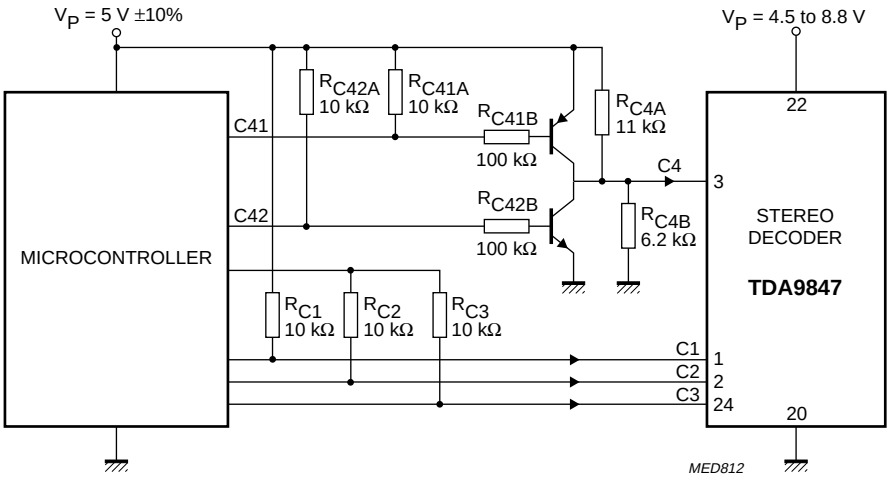


Fig.9 Test circuit for measurement of ripple rejection.



All resistors: ±2%.

Fig.10 Application circuit for the stereo decoder TDA9847 in conjunction with a microcontroller [LOW/HIGH output ports with internal pull-ups or push-pull stages (C1 to C3) and LOW/high-ohmic/HIGH output Port (C4)].

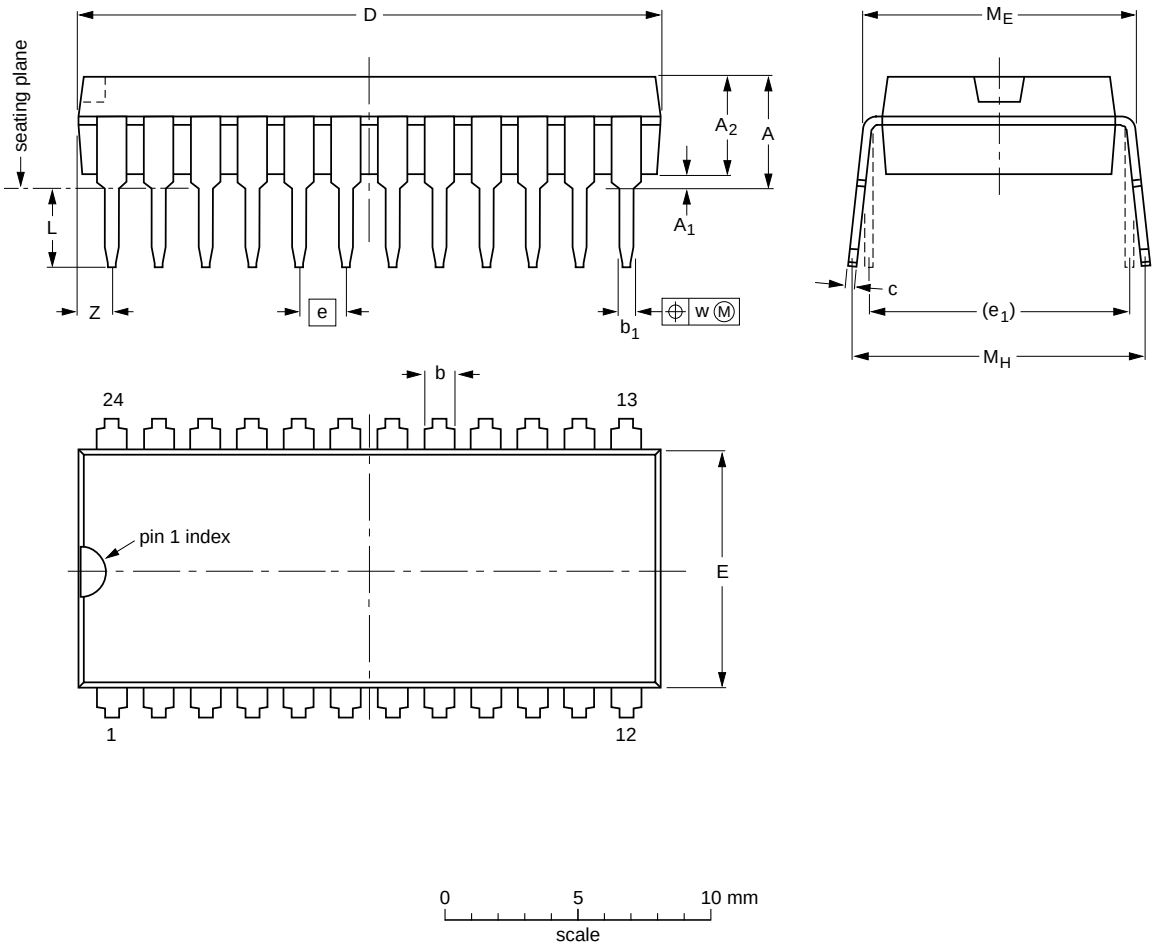


Resistors RC4A and RC4B ±2%; all other resistors ±10%; transistors BC types or equivalent.

Fig.11 Application circuit for the stereo decoder TDA9847 in conjunction with a microcontroller (LOW/HIGH with open-drain output ports).

PACKAGE OUTLINES

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

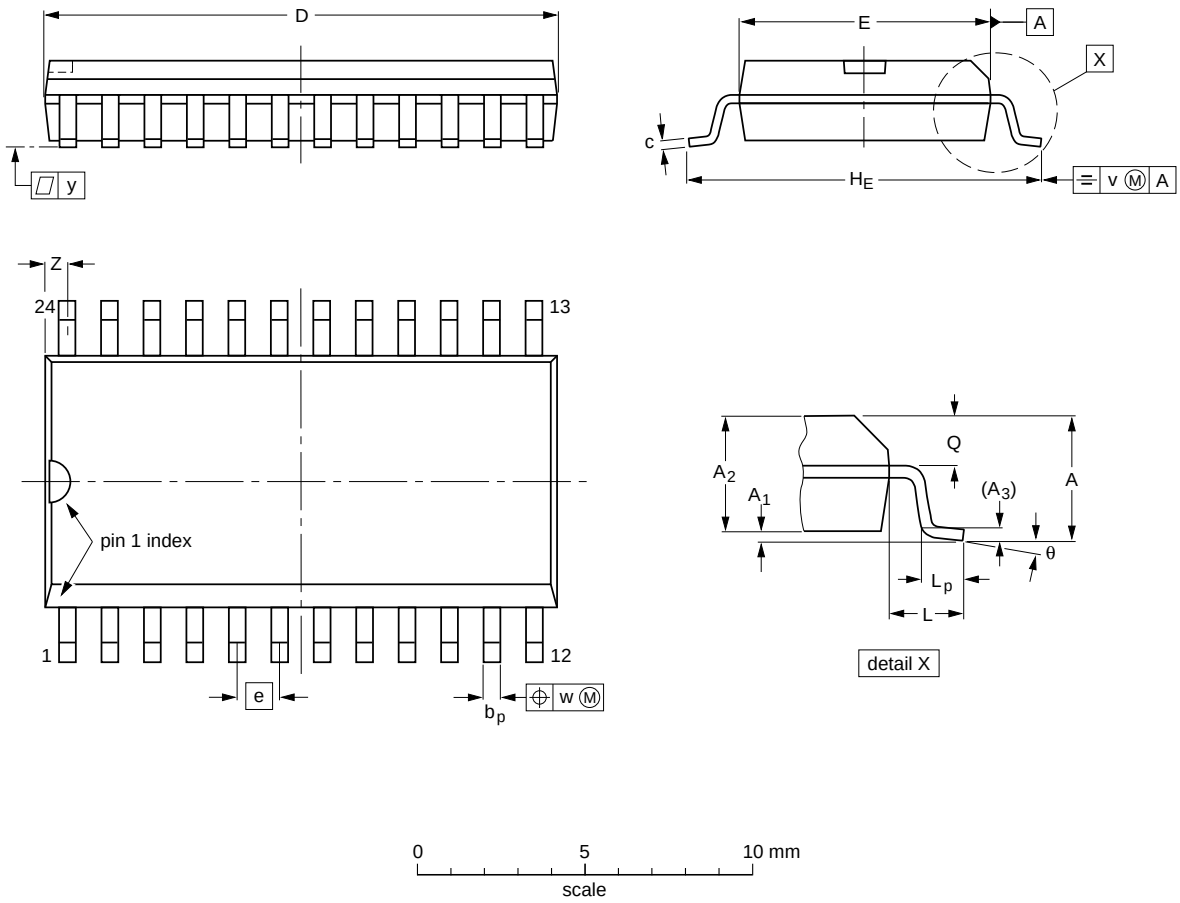
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.